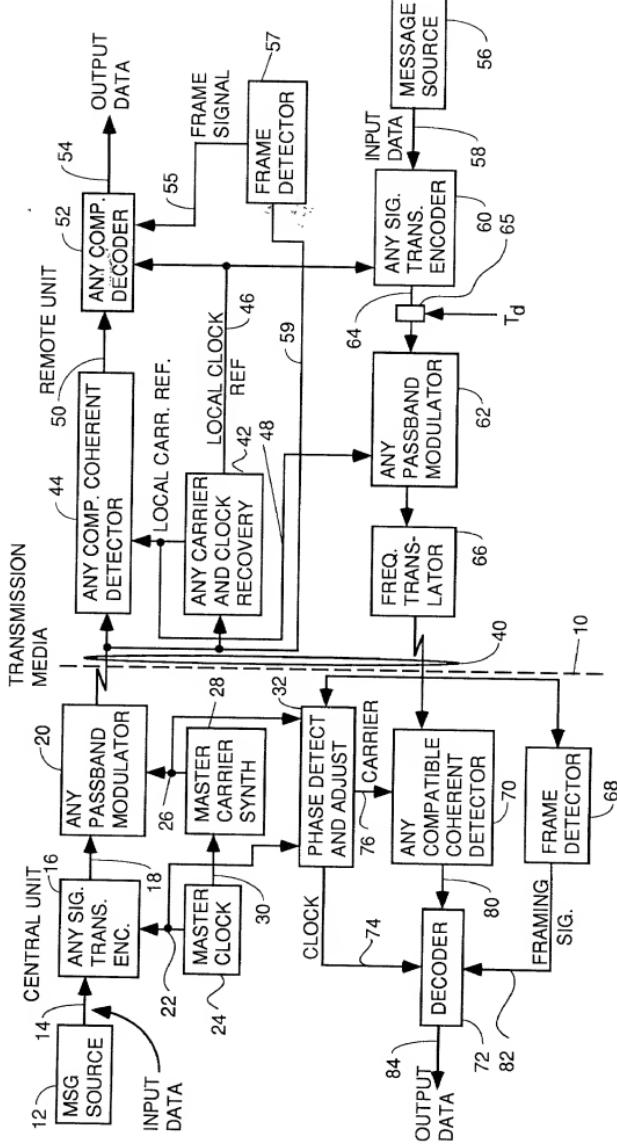


FIG. 1



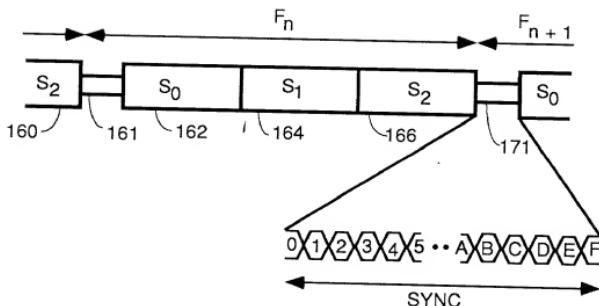


FIG. 2A

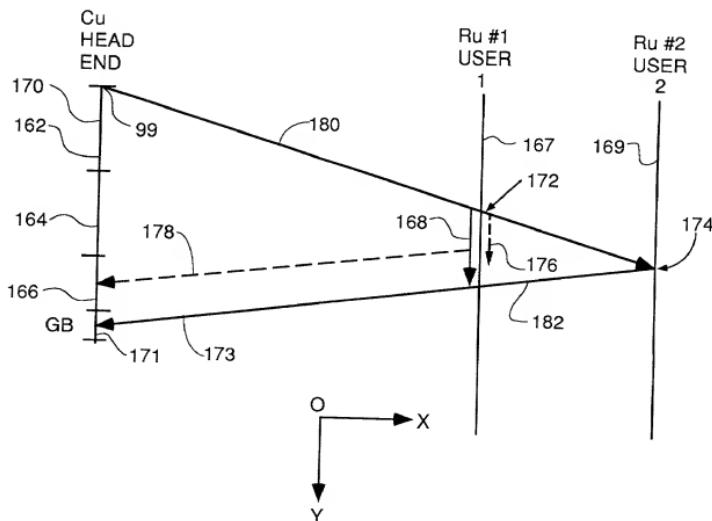
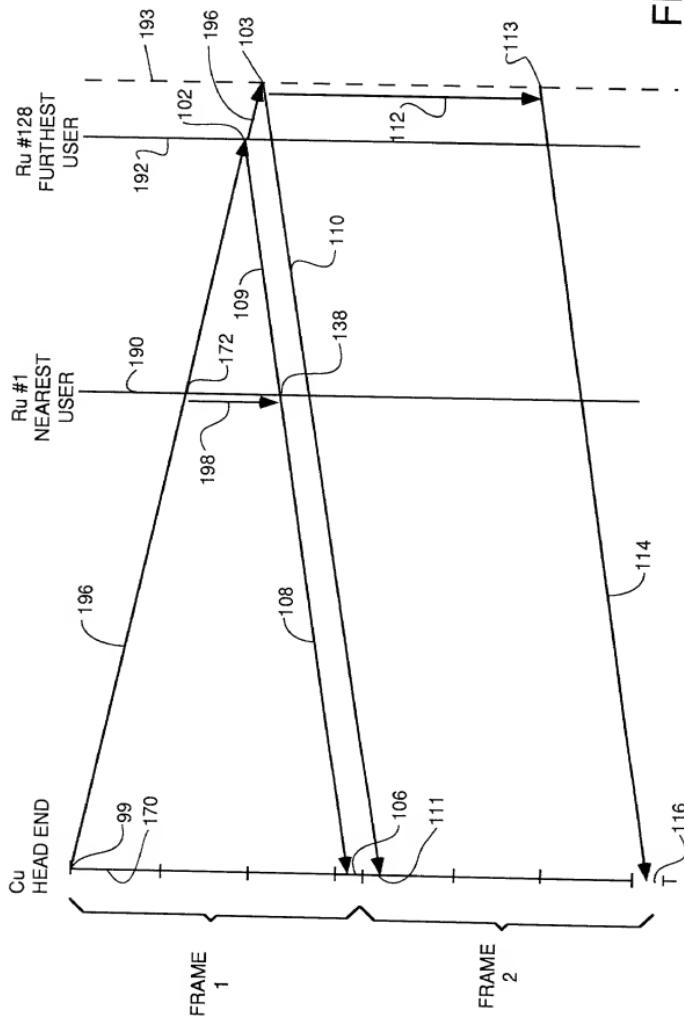


FIG. 2B

FIG. 3



TRUNKING "ECE 49360

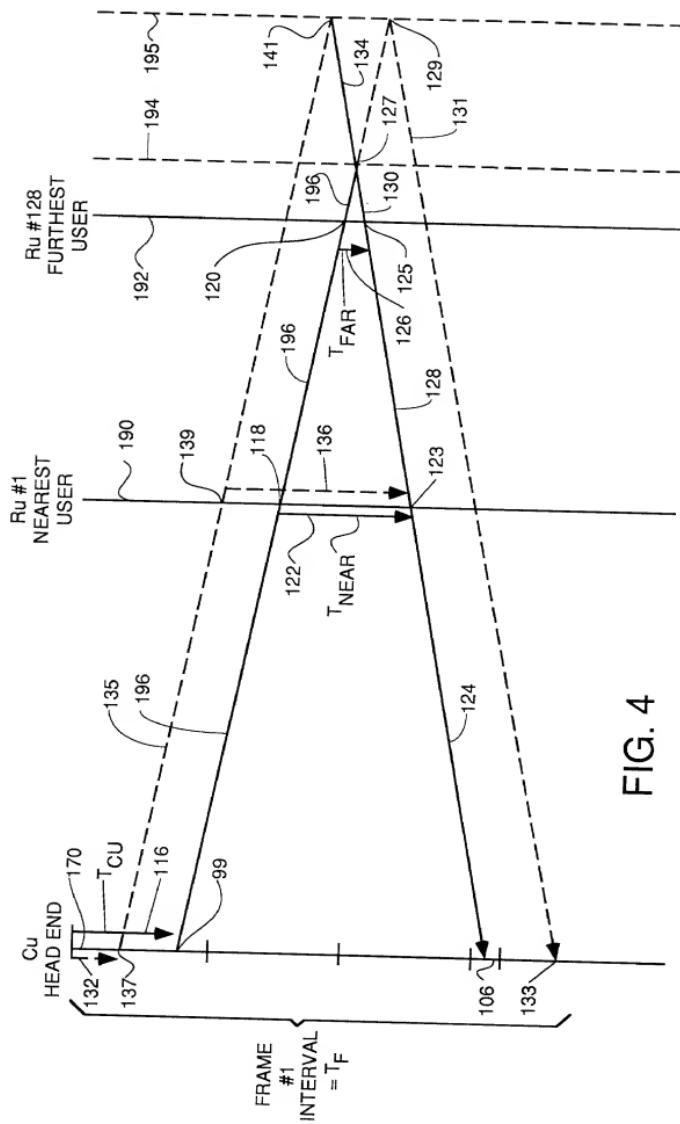
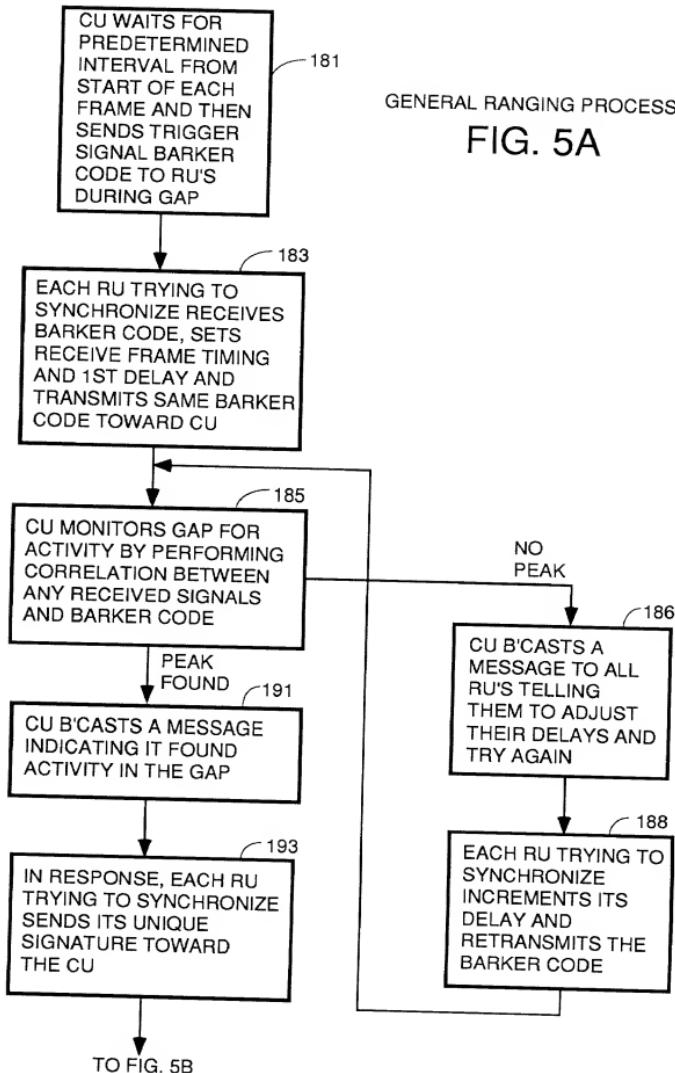


FIG. 4



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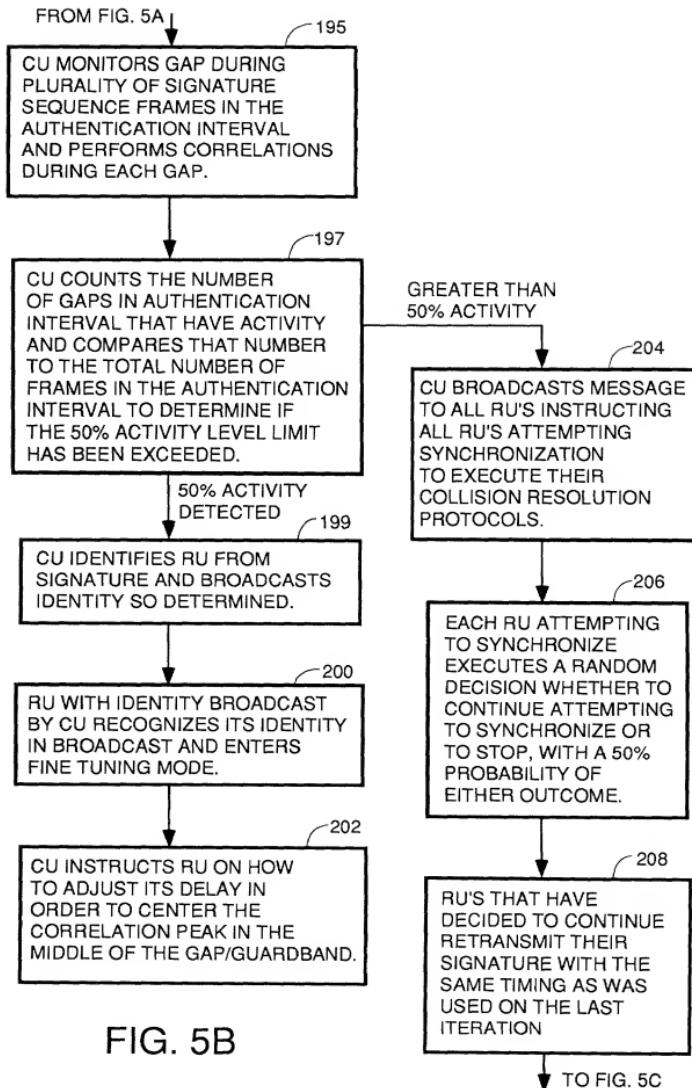


FIG. 5B

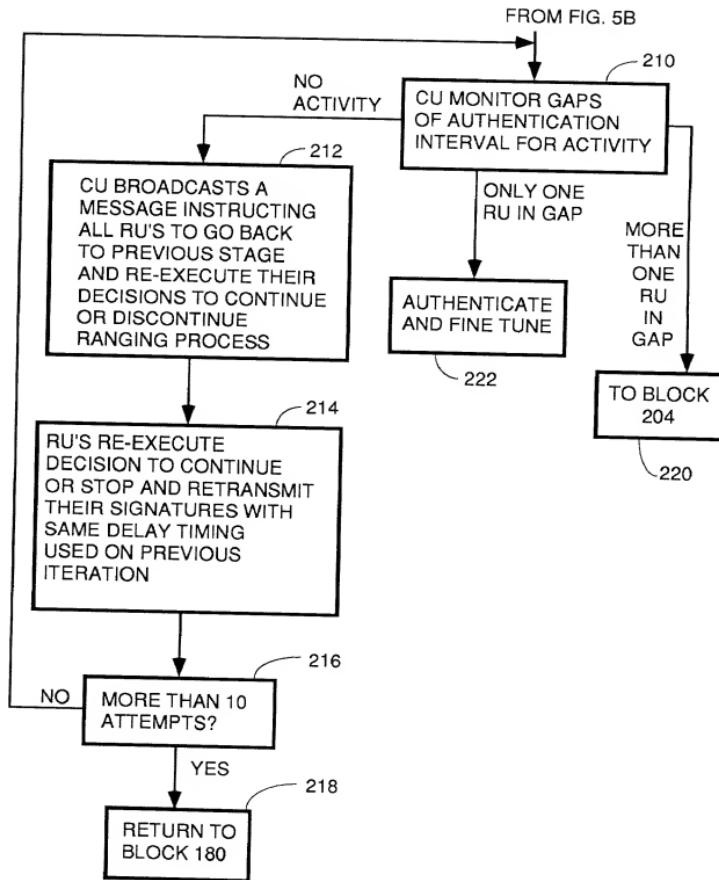


FIG. 5C

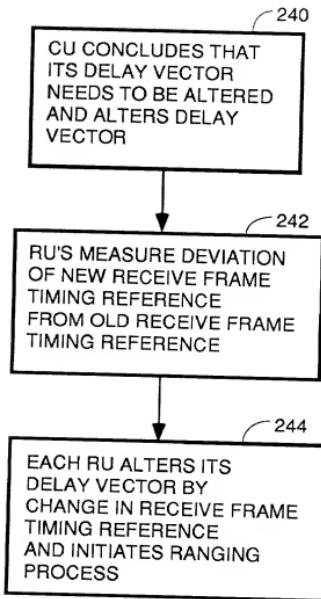


FIG. 6
DEAD RECKONING RE-SYNC

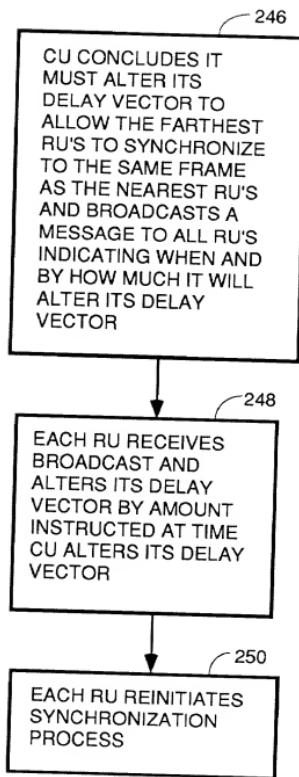
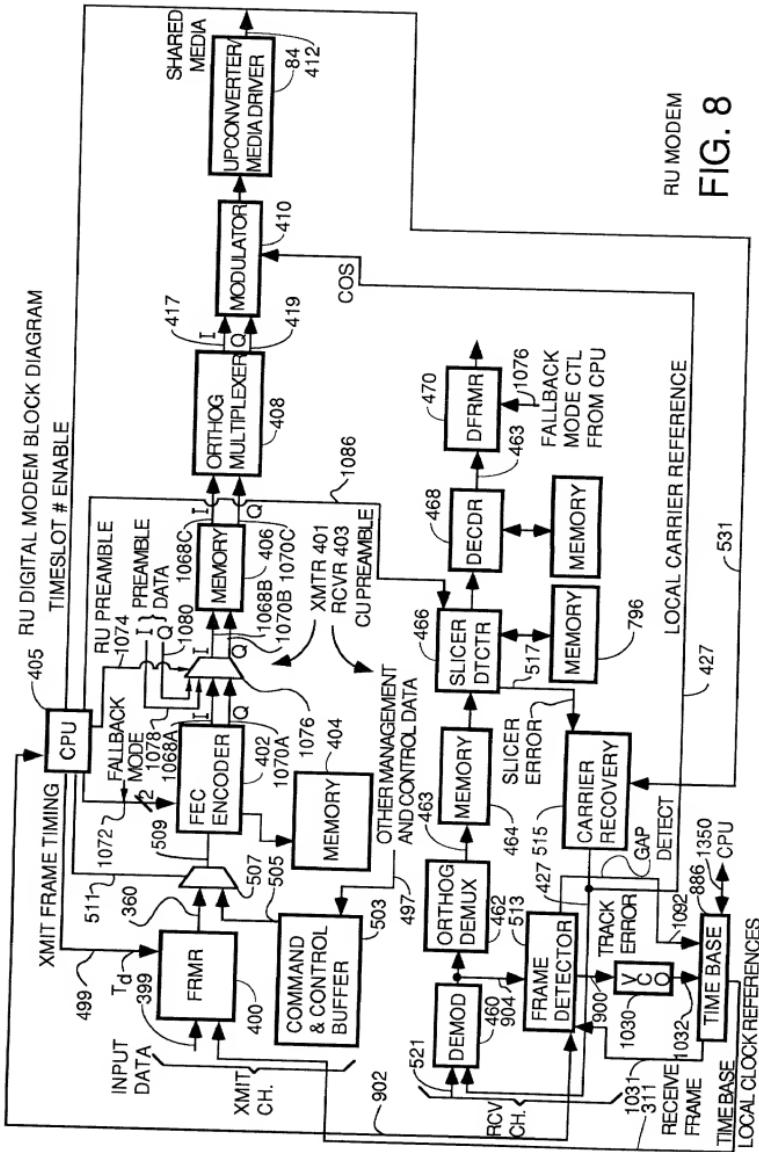


FIG. 7
PRECURSOR EMBODIMENT

```

    graph TD
        XFT[XMIT FRAME TIMING] --> CPU[CPU]
        XFT --> DMD[DIGITAL MODEM BLOCK DIAGRAM]
        CPU --> DMD
        DMD --> TS[TIMESLOT # ENABLE]
        DMD --> RUDM[RU DIGITAL MODEM]
        RUDM --> TS
    
```



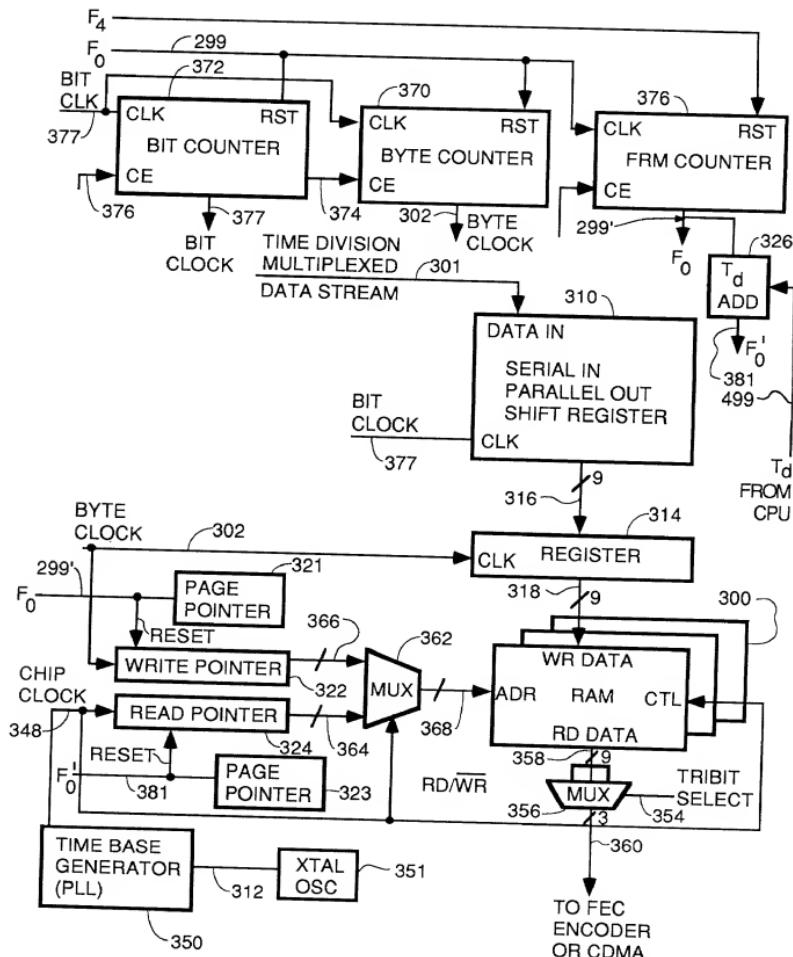


FIG. 9

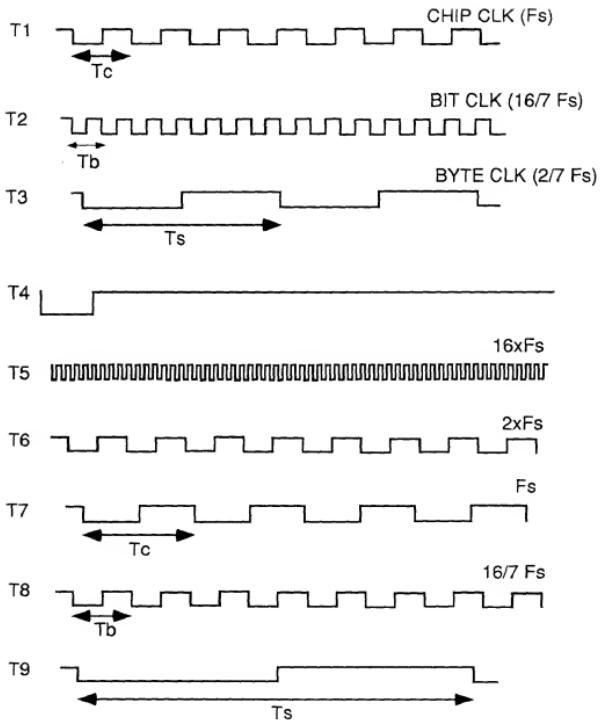


FIG. 10

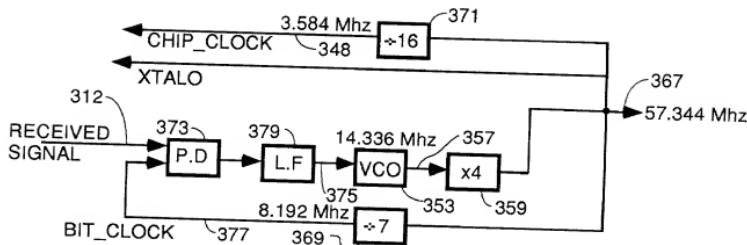


FIG. 11

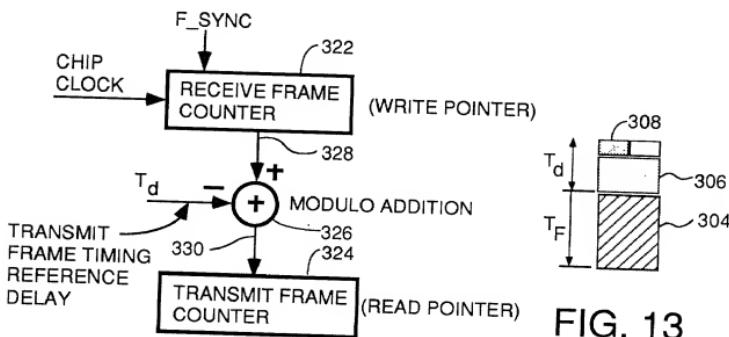


FIG. 13

FIG. 12

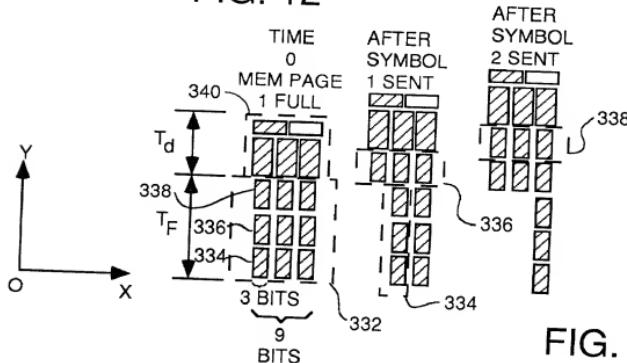


FIG. 14

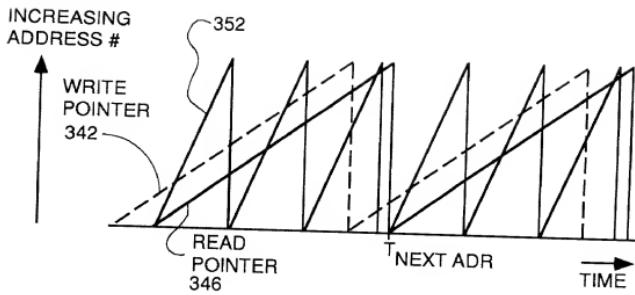


FIG. 15

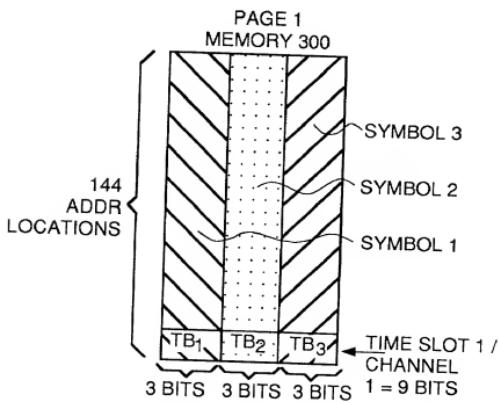
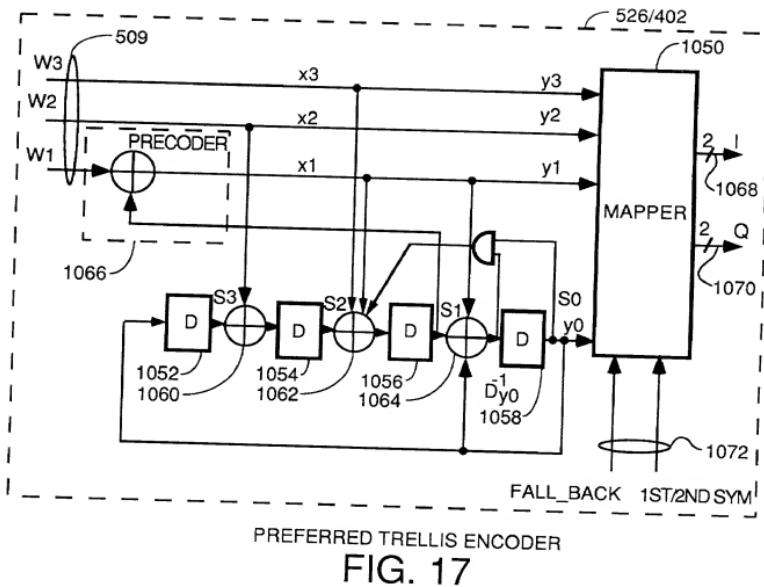


FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17

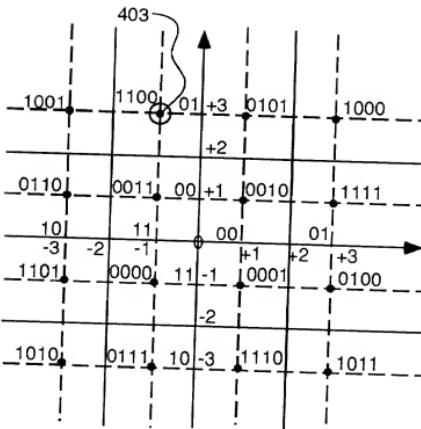


FIG. 18

0000	111	111	
0001	001	111	$= 1 - j$
0010	001	001	$= 1 + j$
0011	111	001	$= -1 + j$
0100	011	111	$= 3 - j$
0101	001	011	$= 1 + 3*j$
0110	101	001	$= -3 + j$
0111	111	101	$= -1 - 3*j$
1000	011	011	$= +3 + 3*j$
1001	101	011	$= -3 + 3*j$
1010	101	101	$= -3 - 3*j$
1011	011	101	$= 3 - 3*j$
1100	111	011	$= -1 + 3*j$
1101	101	111	$= -3 - j$
1110	001	101	$= 1 - 3*j$
1111	011	001	$= 3 + j$

403

FIG. 19

INFORMATION
VECTOR [B]
FOR EACH
SYMBOL

ORTHOGONAL
CODE MATRIX

$$\begin{array}{l}
 483 \\
 481
 \end{array} \times \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ \vdots & & & \end{bmatrix} \times \begin{bmatrix} c_{1,1} & c_{1,2} & \cdots & c_{1,144} \\ c_{2,1} & c_{2,2} & \cdots & c_{2,144} \\ \vdots & \vdots & & \vdots \end{bmatrix}$$

FIG. 20A

REAL
PART OF
INFO
VECTOR
[b] FOR
FIRST
SYMBOL

405

$$\begin{bmatrix} +3 \\ -1 \\ -1 \\ +3 \end{bmatrix} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ -1 & 1 & -1 & 1 \\ -1 & 1 & 1 & -1 \end{bmatrix} = \begin{bmatrix} 4 \\ 0 \\ 0 \\ -8 \end{bmatrix} \quad 409$$

REAL
PART OF
RESULT
VECTOR

407

$[b_{\text{REAL}}] \times [\text{CODE MATRIX}] = [R_{\text{REAL}}] = \text{"CHIPS OUT" ARRAY-REAL}$

FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

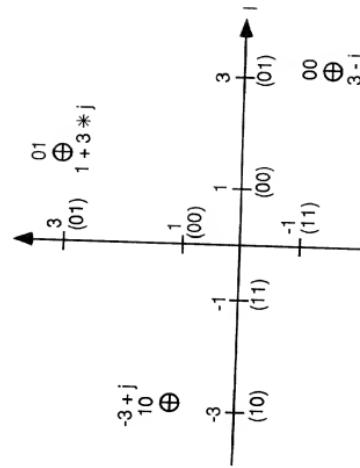


FIG. 21

LSBs y ¹ y ⁰	PHASE 1+Q	MSBs y ³ y ² (2nd 1st symbol)	PHASE difference 1+Q WHEN LSB=00	1+Q WHEN LSB=01	1+Q WHEN LSB=10	1+Q WHEN LSB=11
00	0	3-j	0	3-j	1+3	-3+j
01	90	1+3	01	90	1+3	-3+j
10	180	-3+j	10	180	-3+j	-1-3
11	-90	-1-3	11	-90	-1-3	3-j

LSB & MSB FALBACK MODE MAPPINGS

FIG. 22

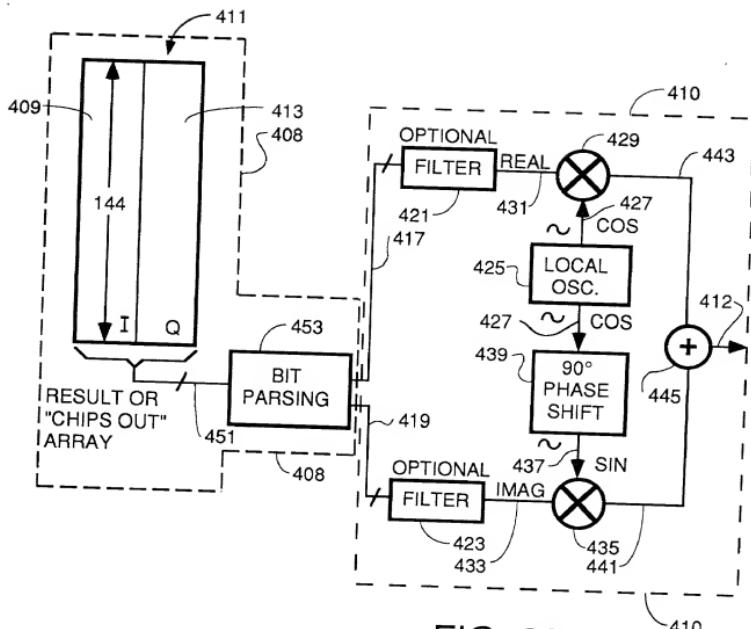


FIG. 23

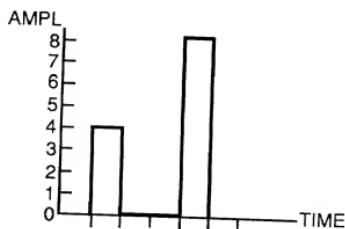


FIG. 24

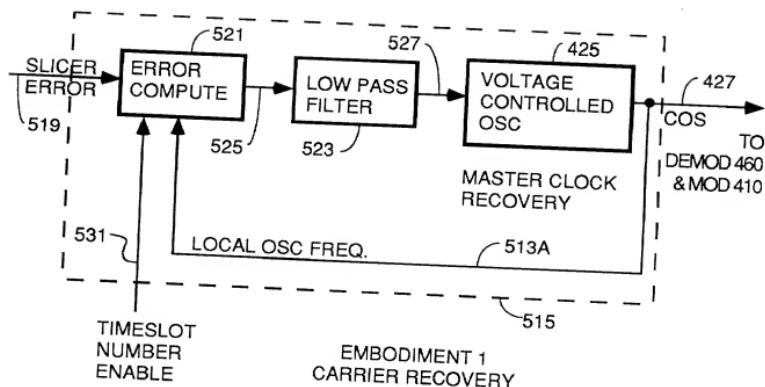


FIG. 25

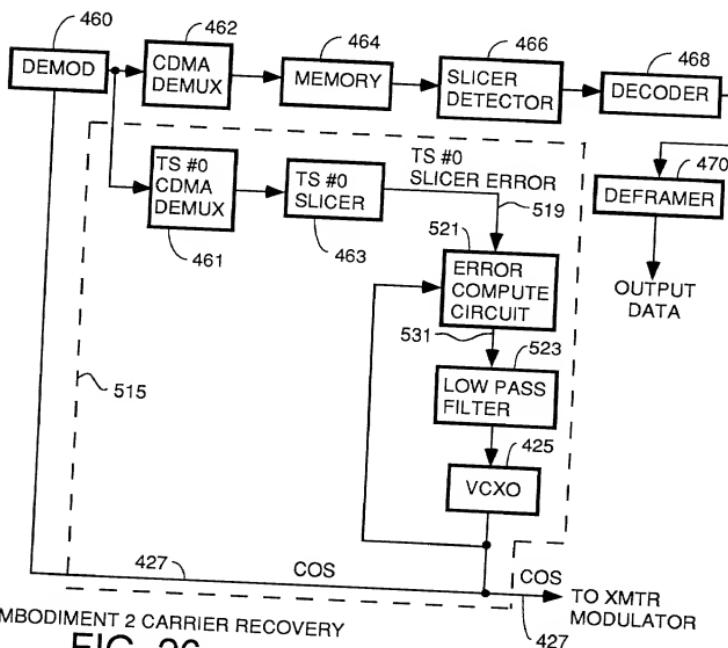


FIG. 26

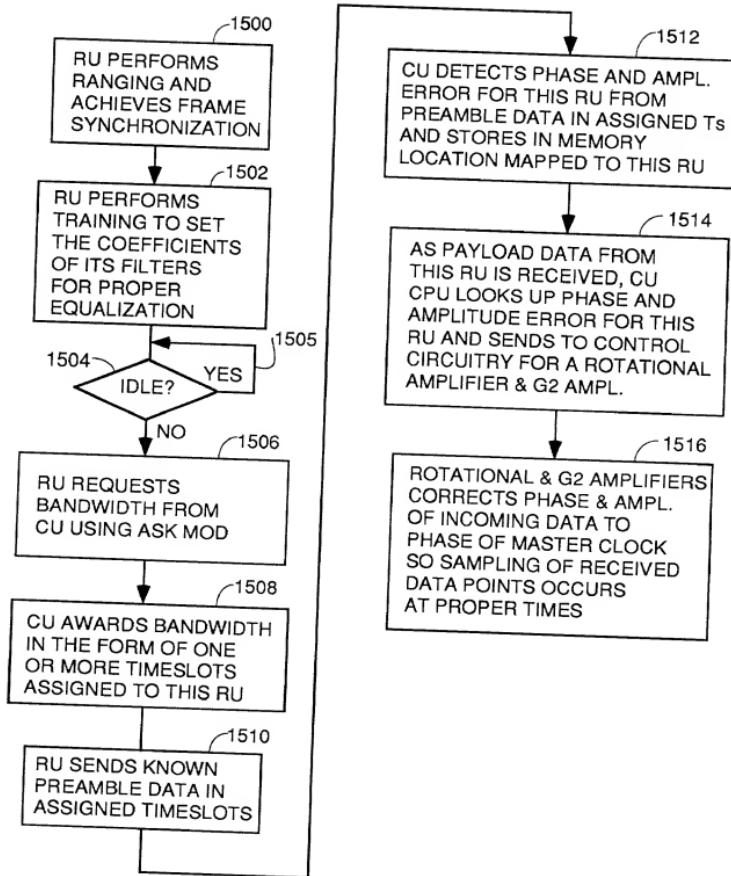
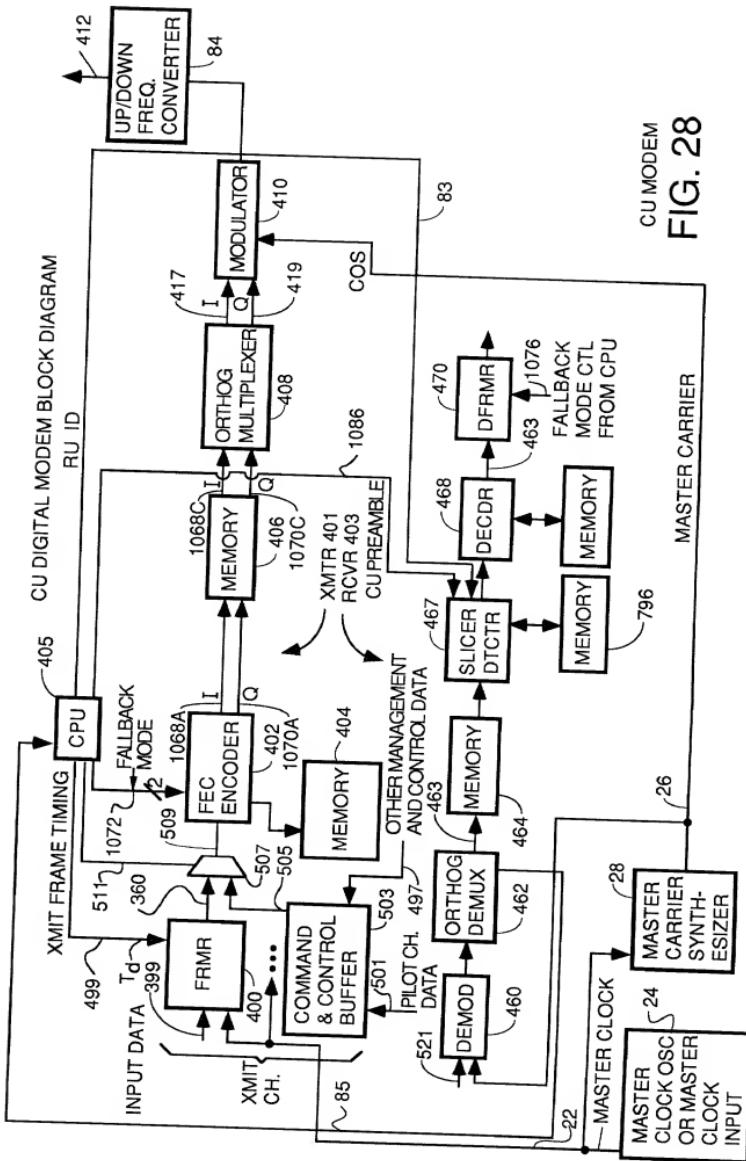


FIG. 27

CU MODEM
FIG. 28



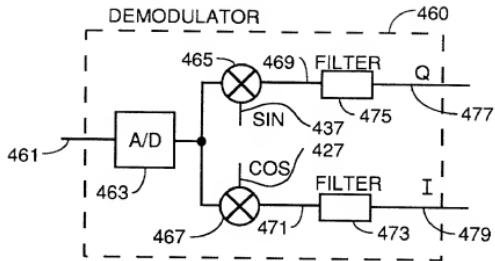


FIG. 29

TOP SECRET//SI EYESAFE

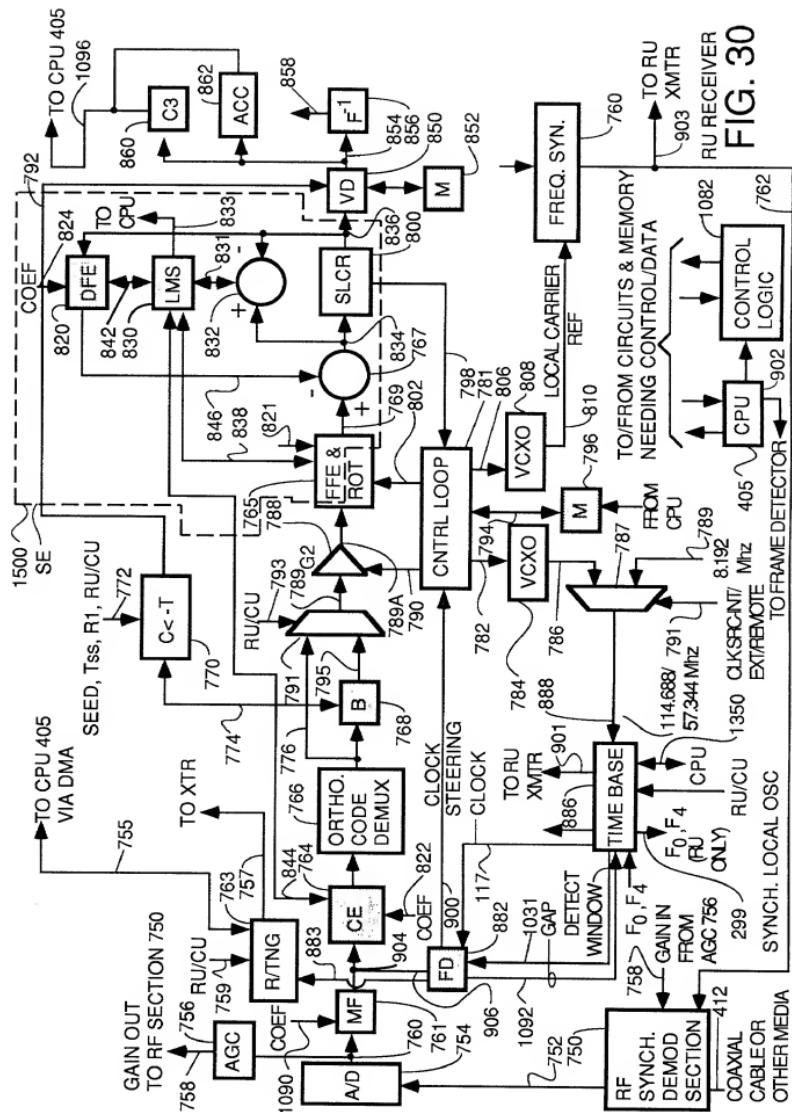
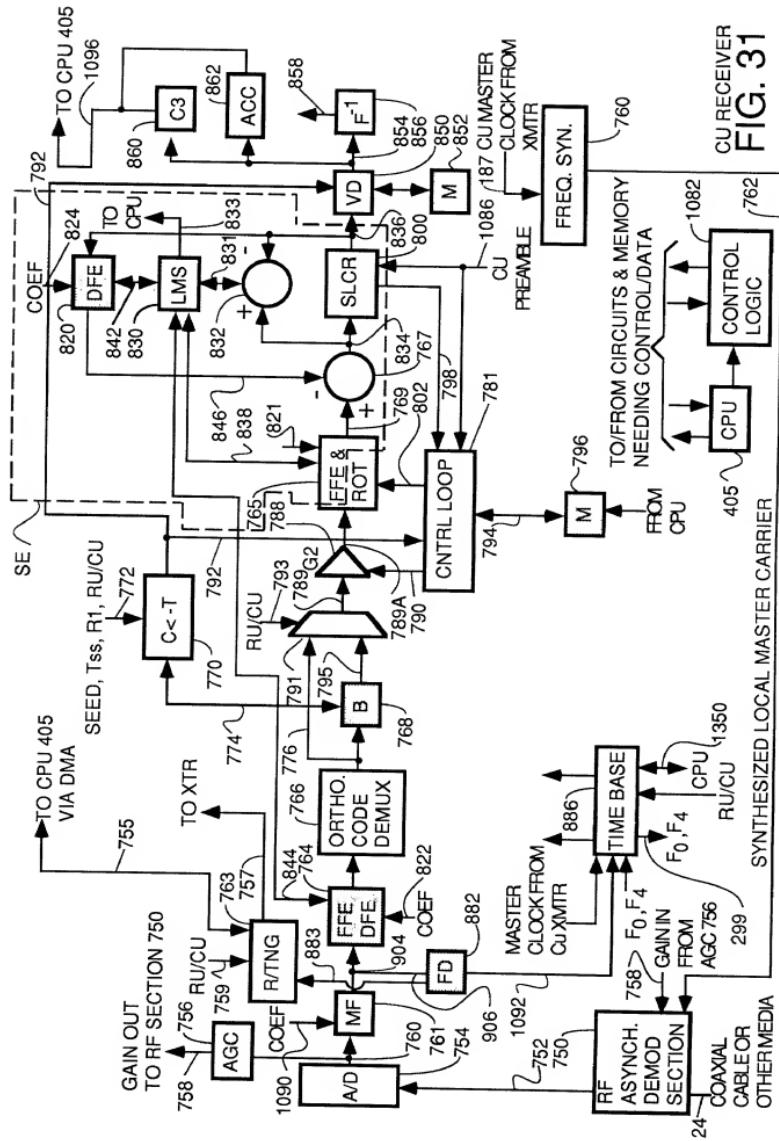
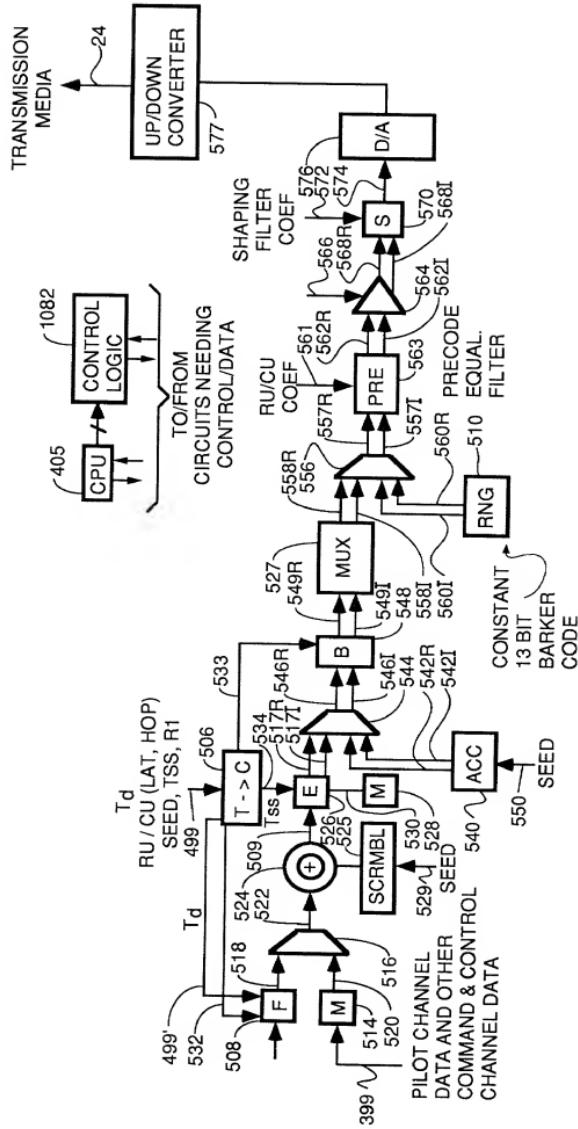


FIG. 30

三九七四三五·052304





CU TRANSMITTER
FIG. 32

卷之三

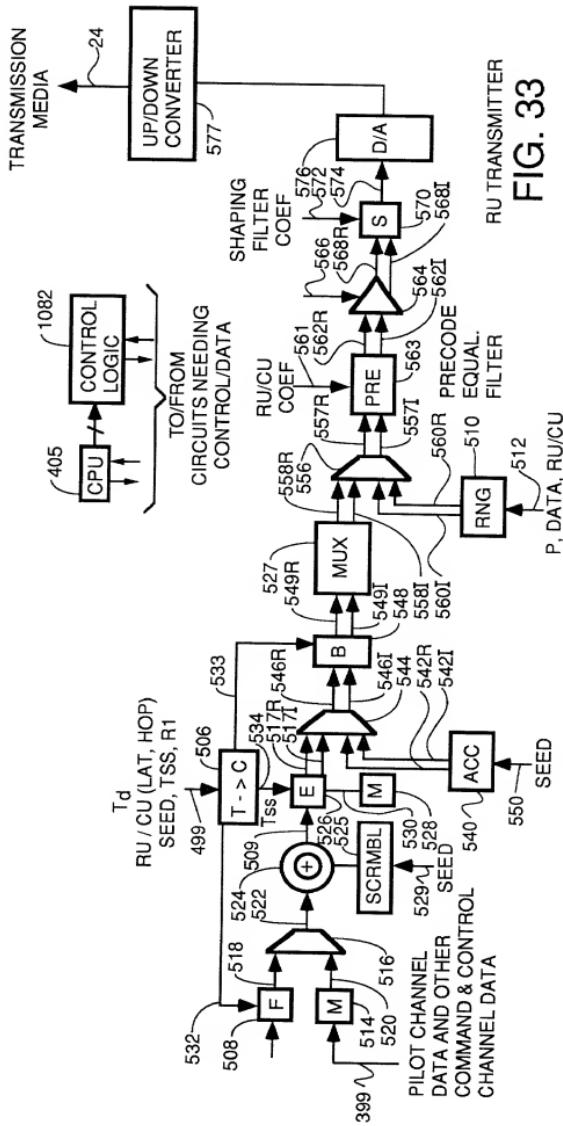


FIG. 33

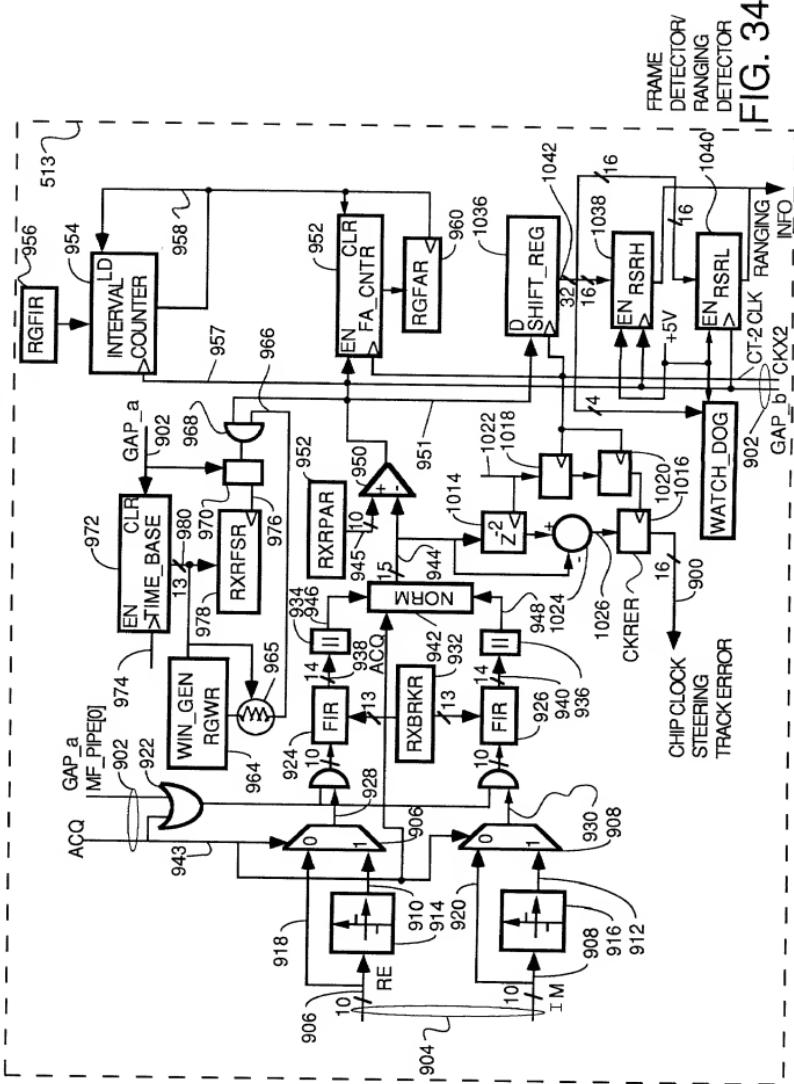


FIG. 34

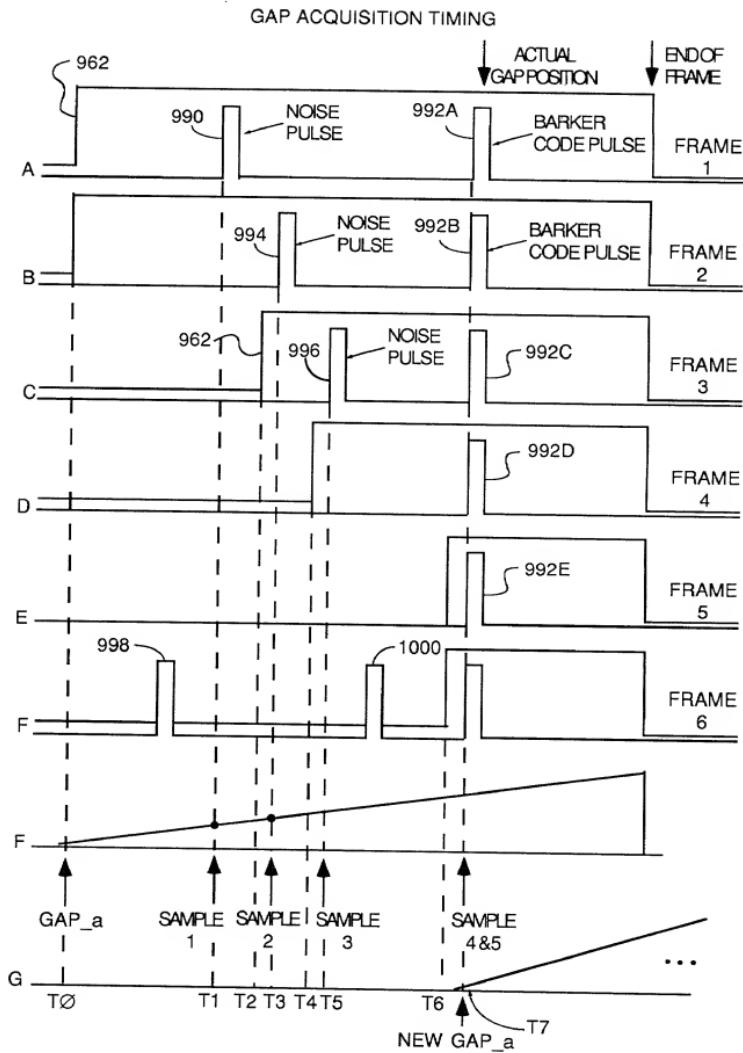


FIG. 35

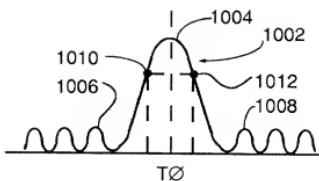


FIG. 36

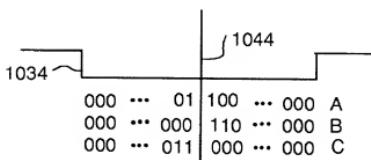


FIG. 37
FINE TUNING TO
CENTER BARKER CODE

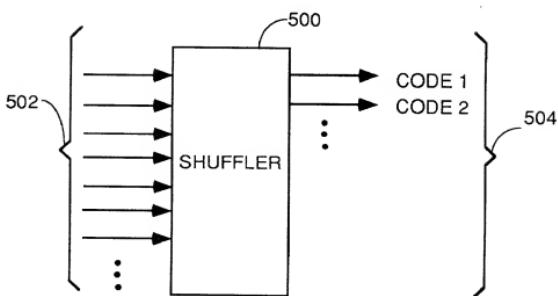
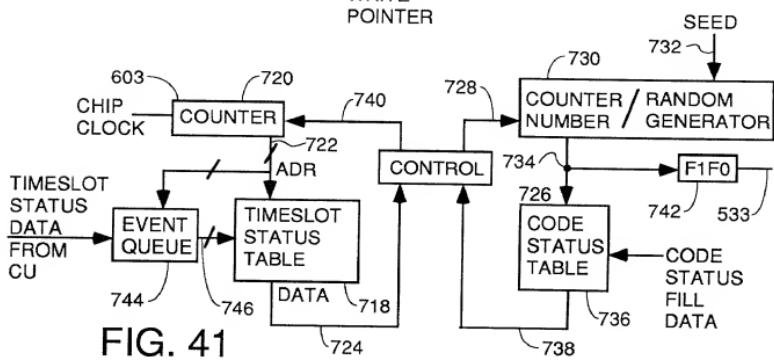
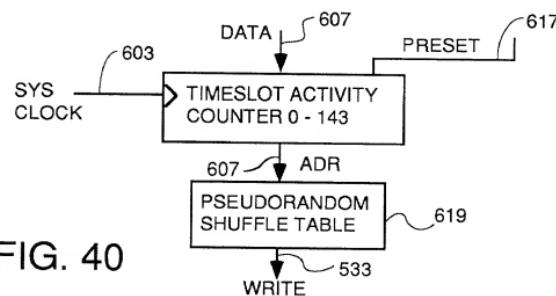
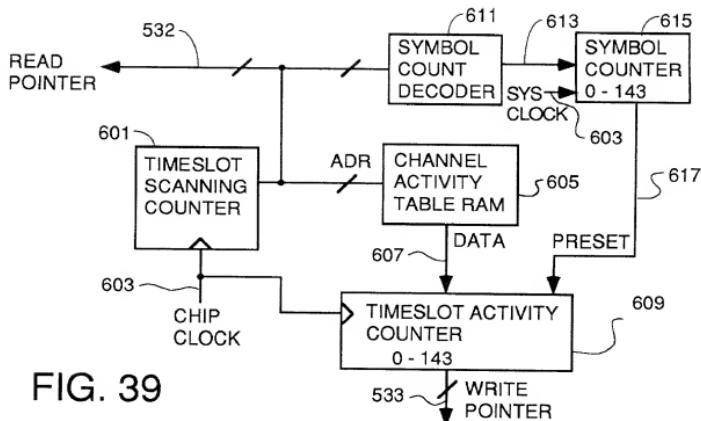


FIG. 38



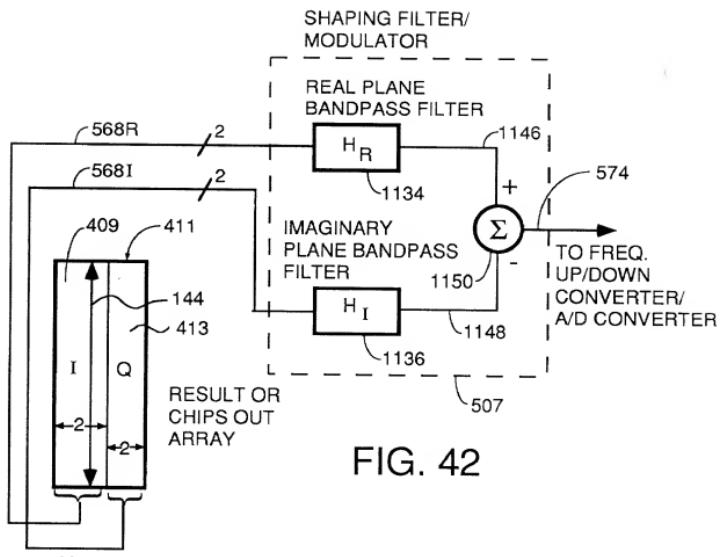


FIG. 42

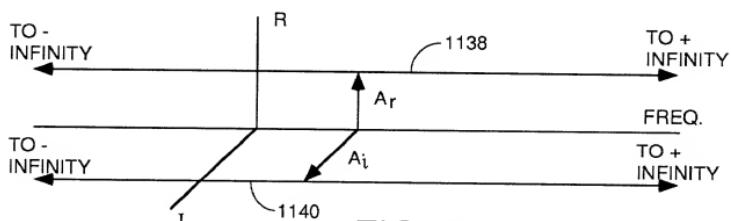


FIG. 43

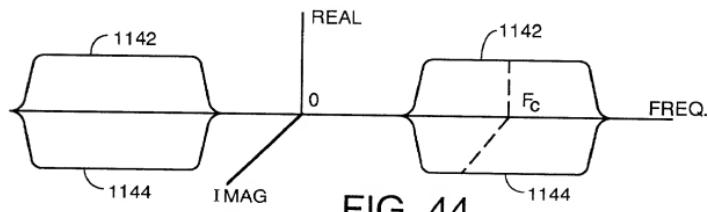
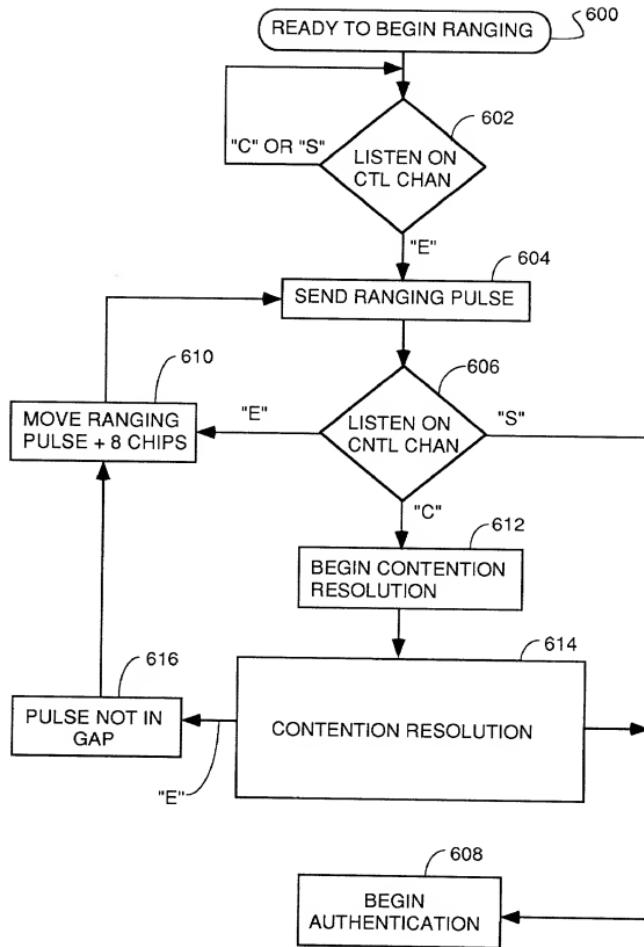
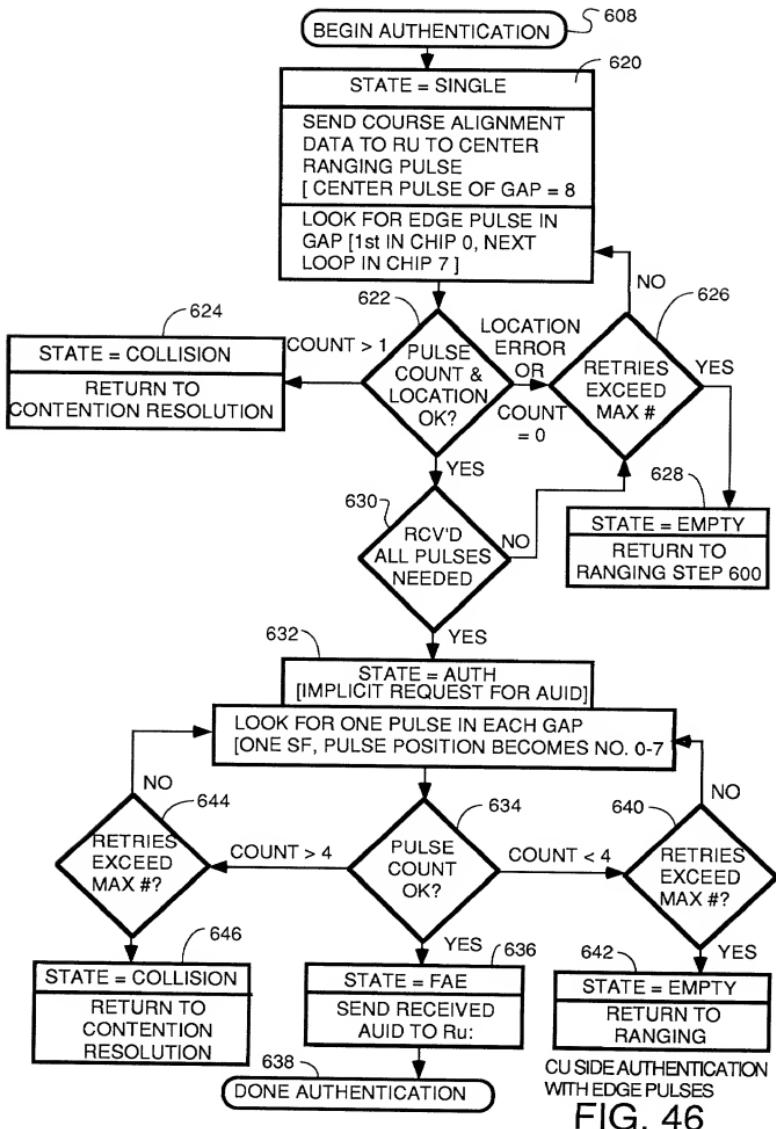
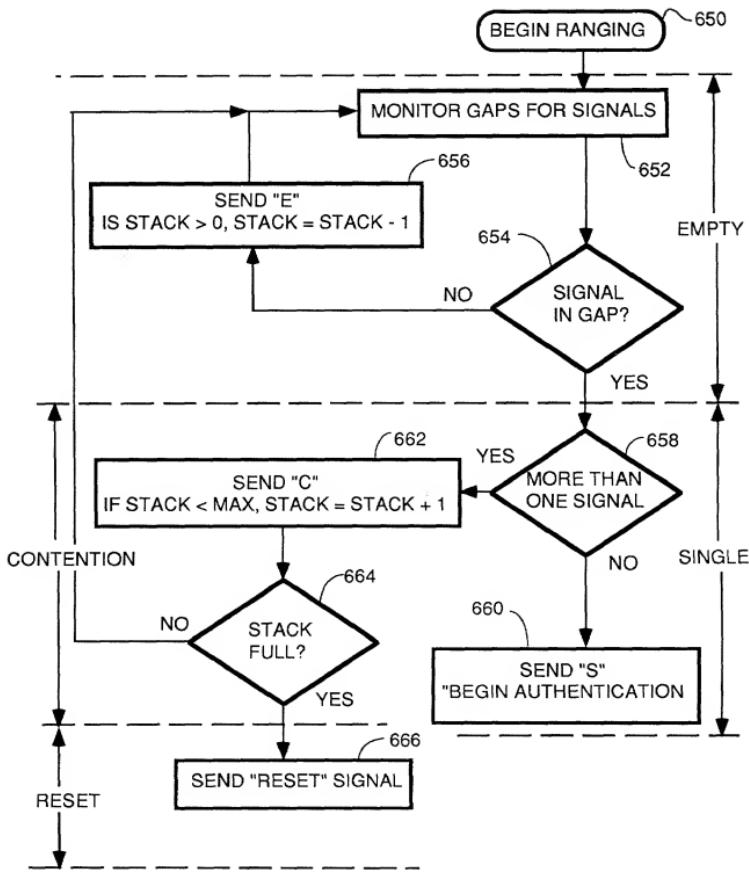


FIG. 44



RU RANGING
FIG. 45

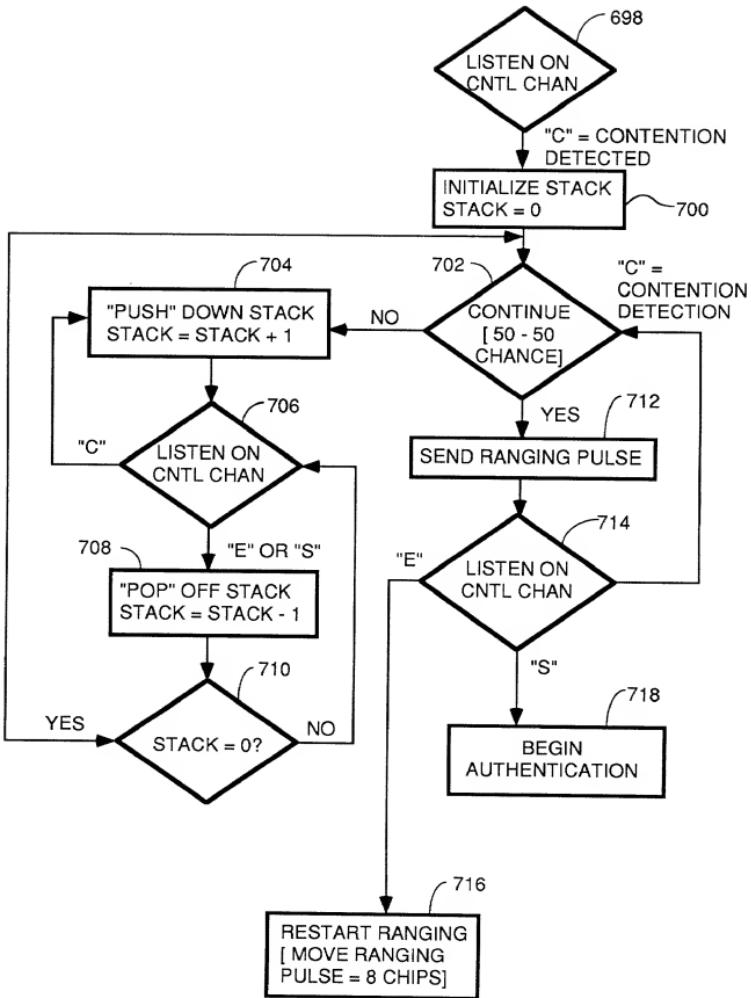




CU RANGING AND CONTENTION RESOLUTION

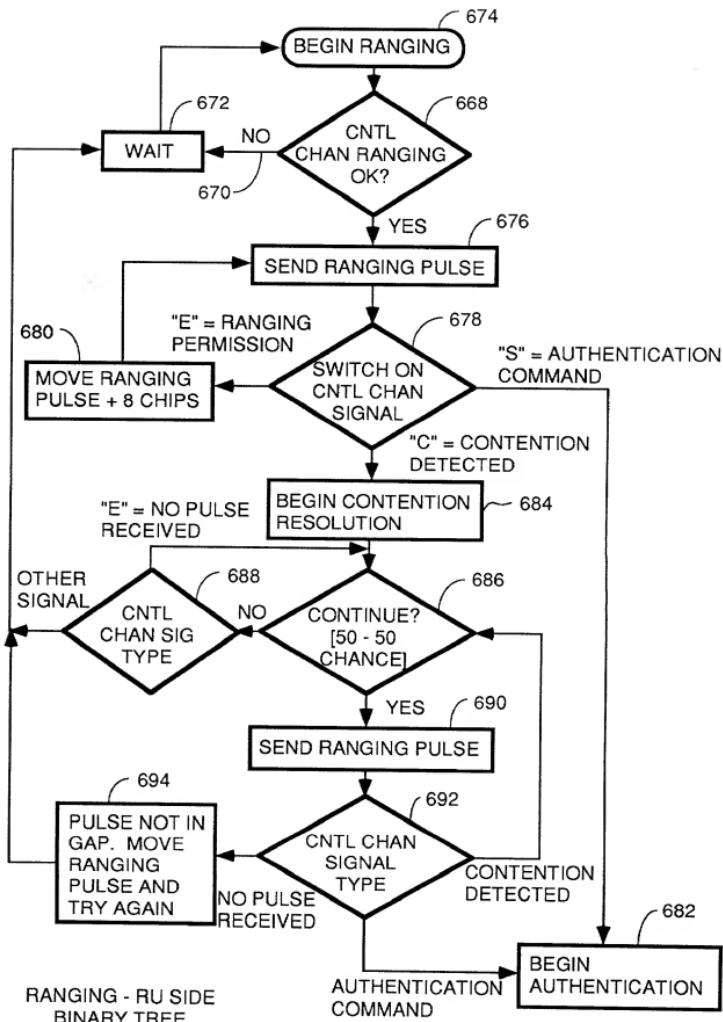
FIG. 47

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CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 48



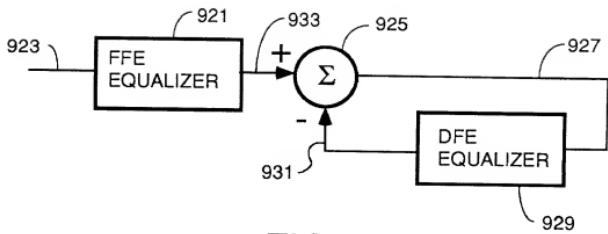


FIG. 50

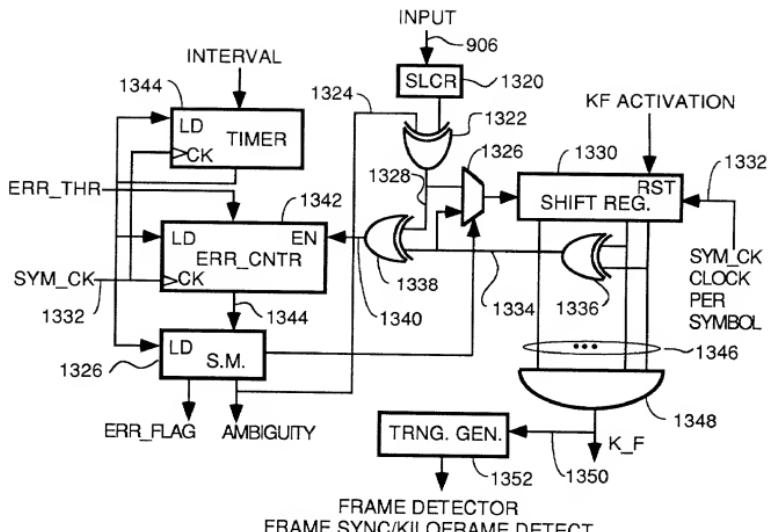
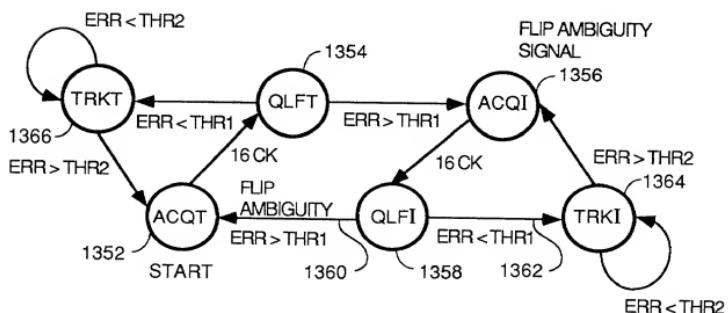
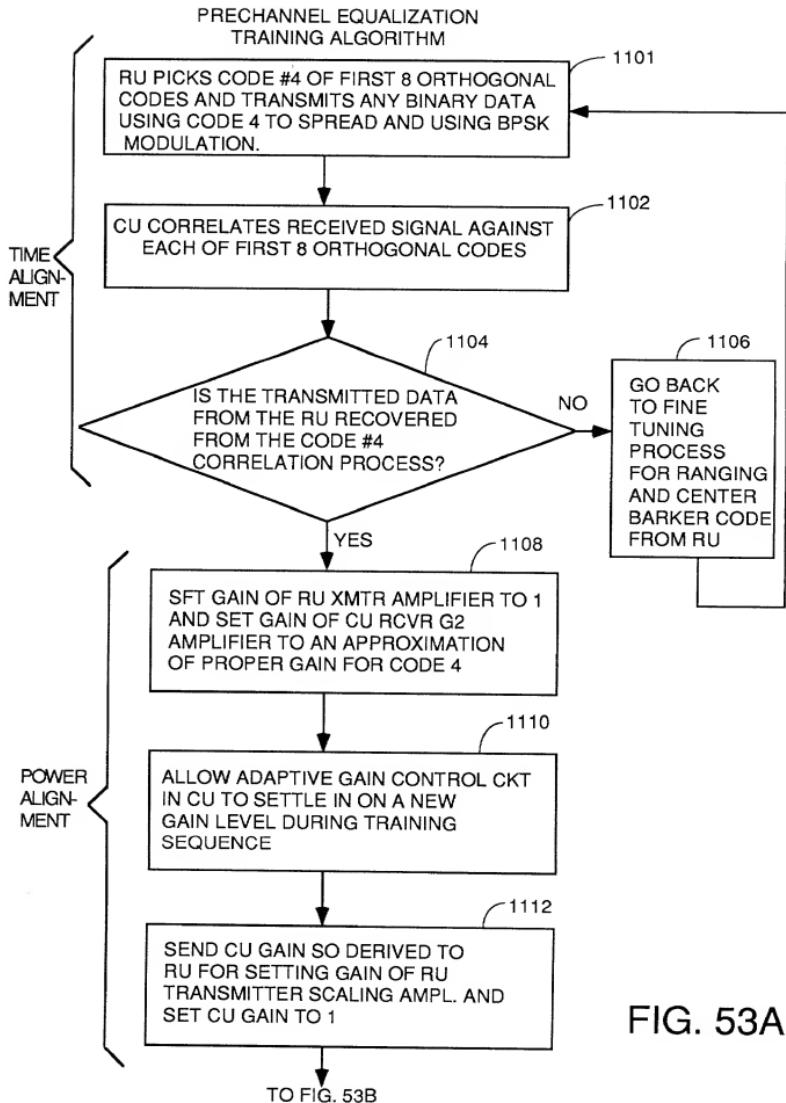


FIG. 51



STATE MACHINE

FIG. 52



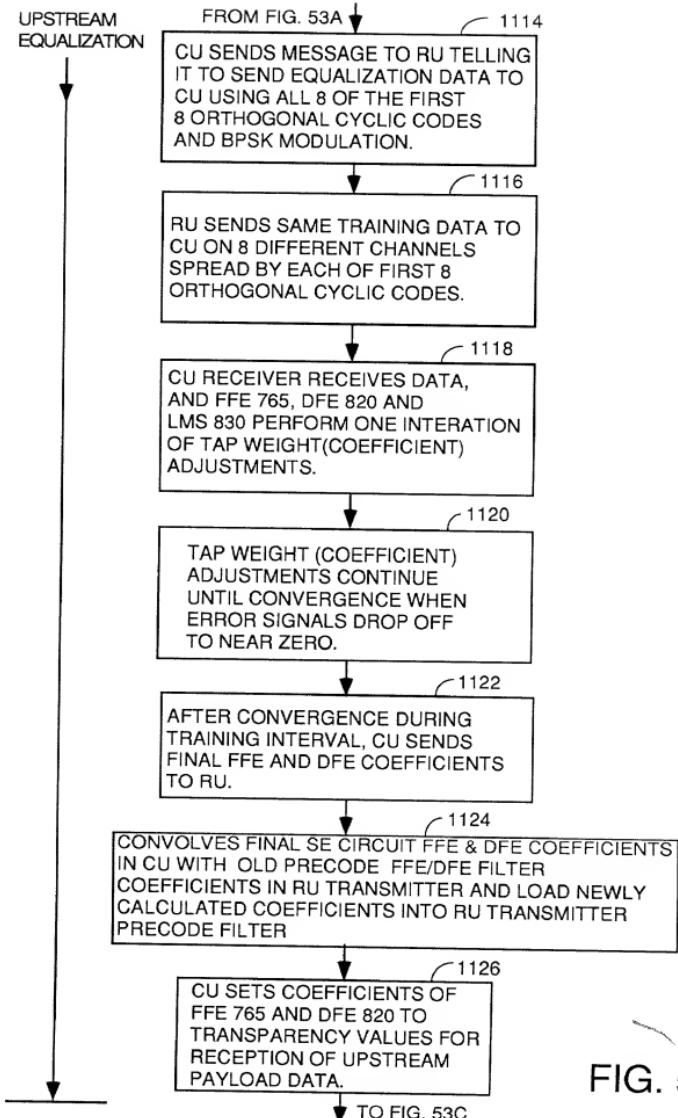


FIG. 53B

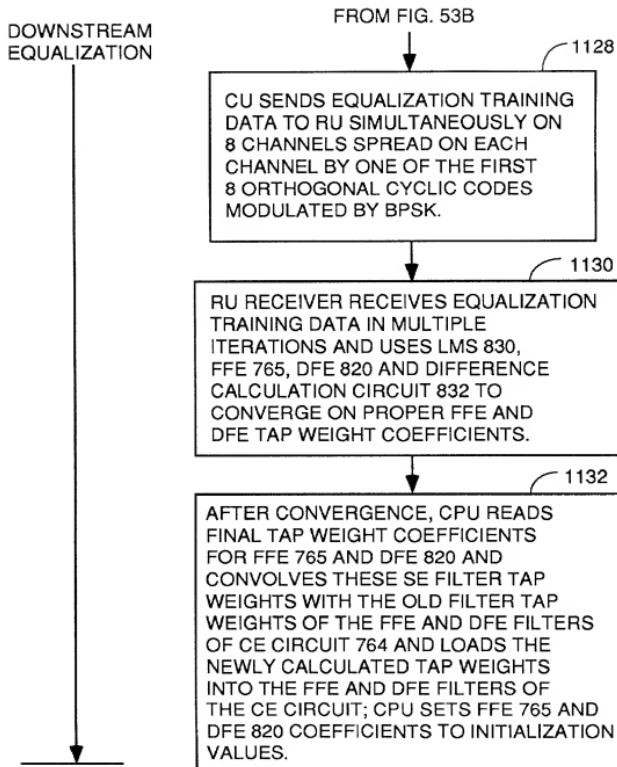


FIG. 53C

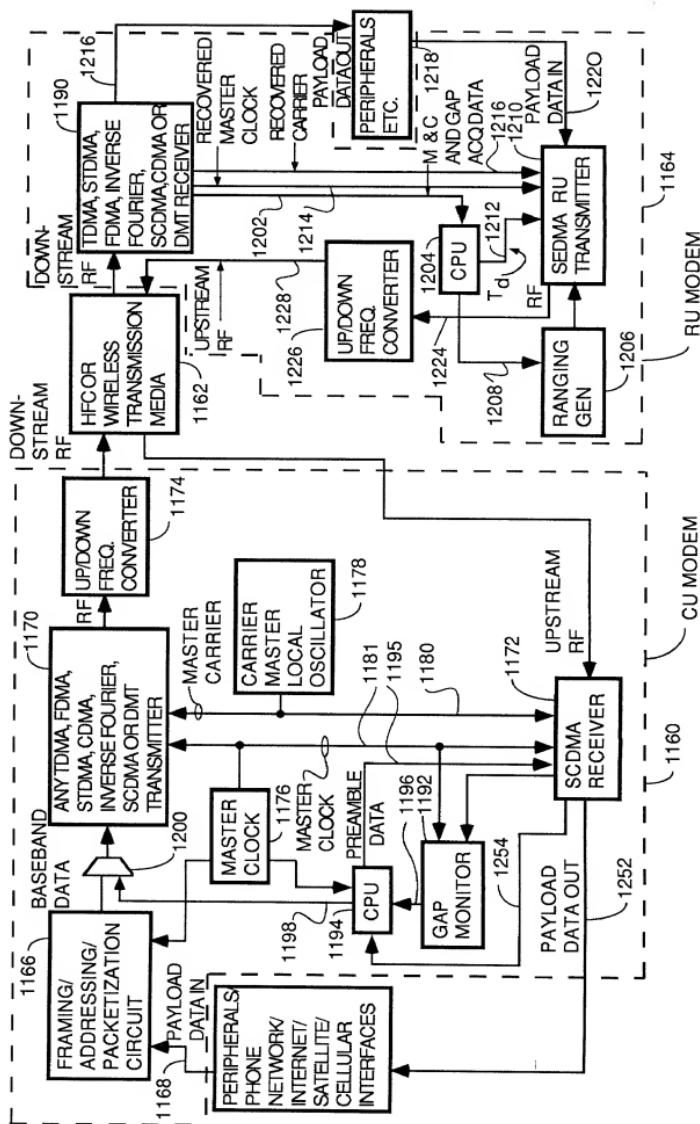
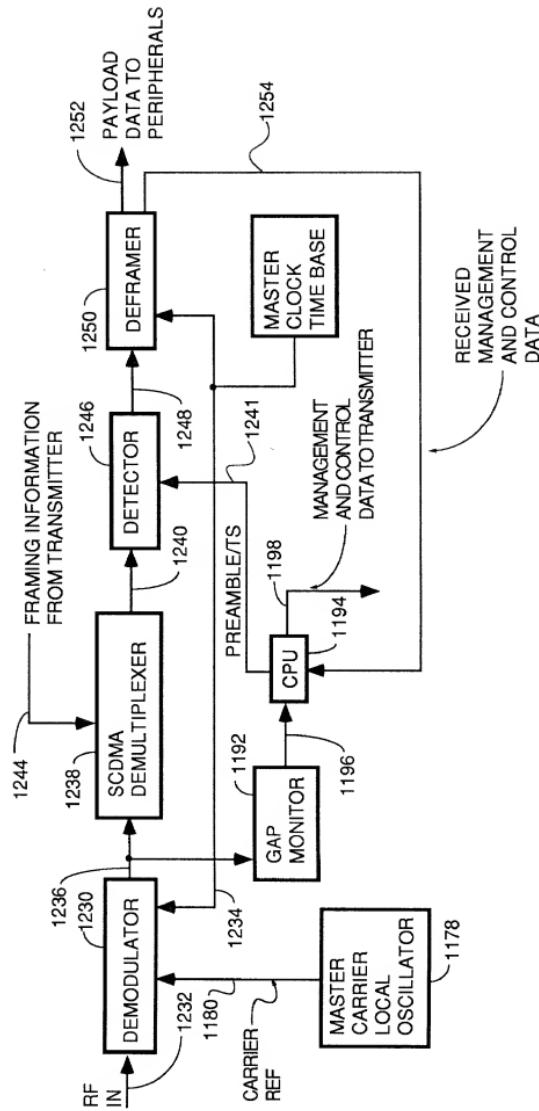


FIG. 54



SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55

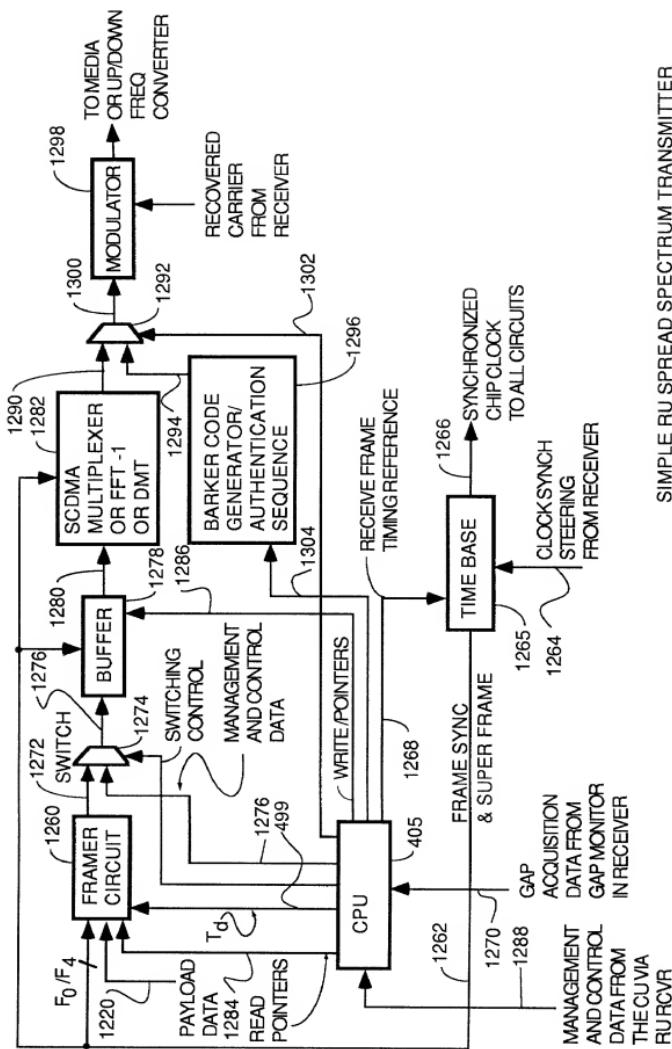


FIG. 56

SIMPLE RRU SPREAD SPECTRUM TRANSMITTER

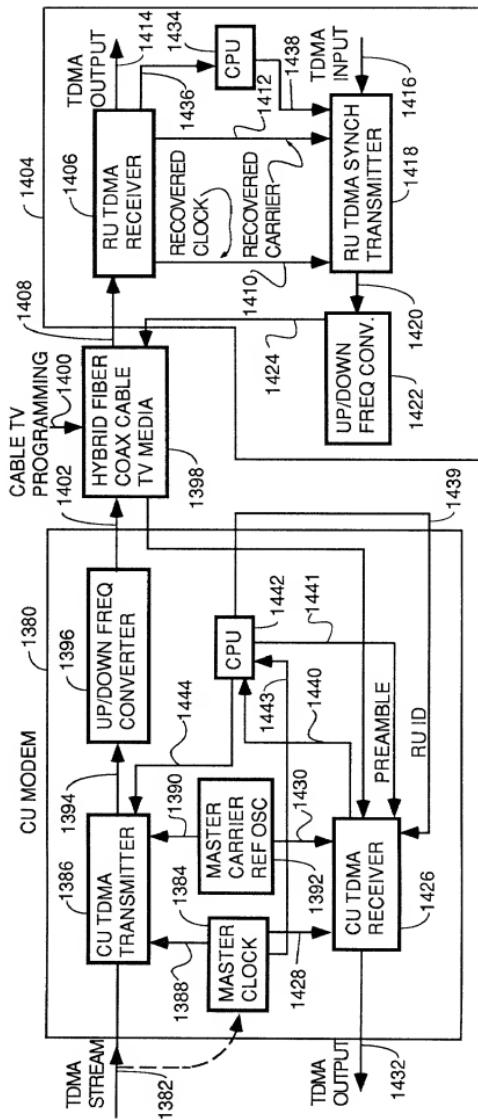


FIG. 57

SYNCHRONOUS TDMA SYSTEM

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OFFSET (CHIPS)	1B ASIC		2A ASIC	
	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

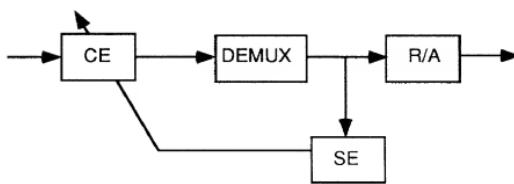
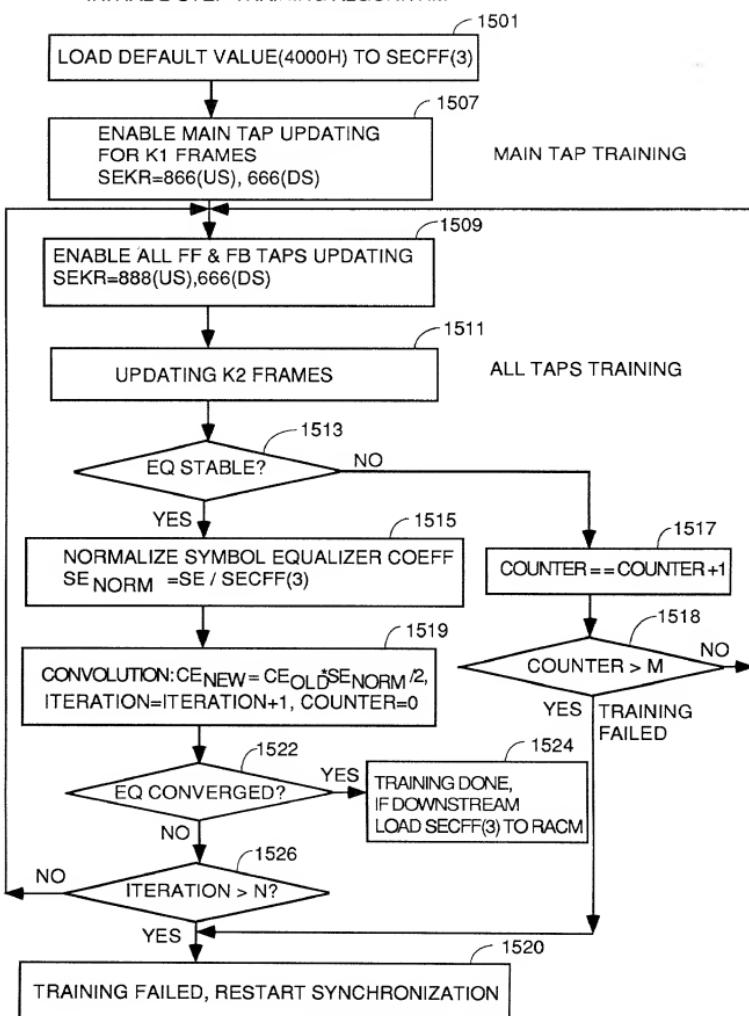


FIG. 59

INITIAL 2-STEP TRAINING ALGORITHM



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

EQ STABILITY CHECK

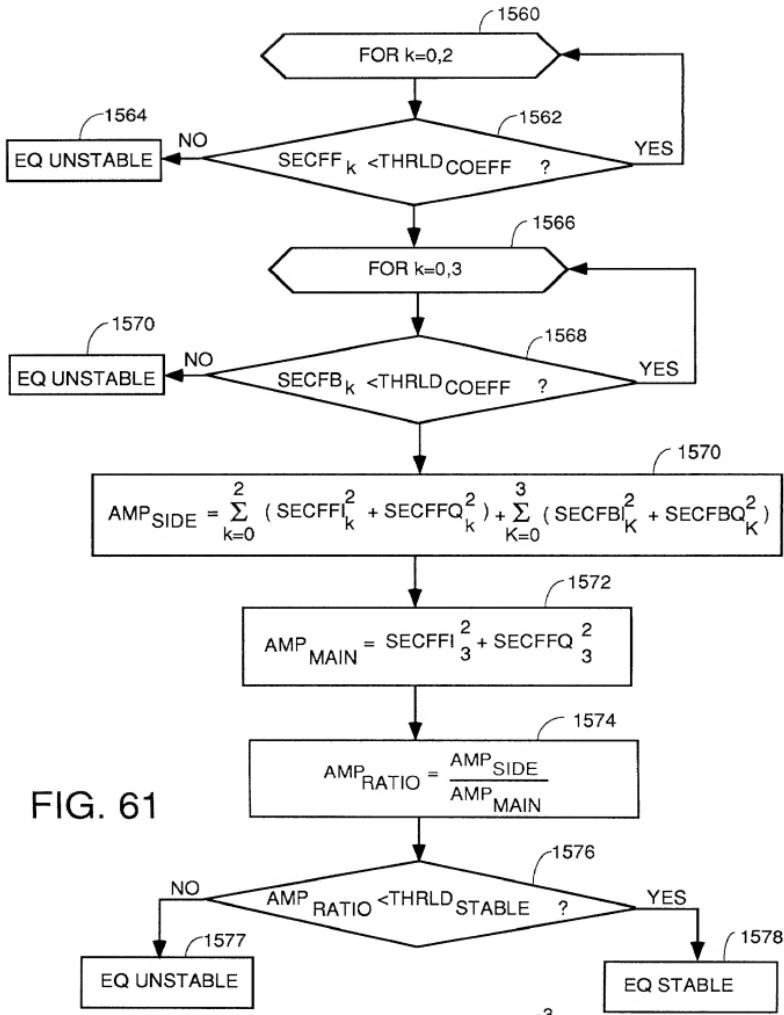


FIG. 61

NOTE: $THRLD_COEFF = 7F00H$ $THRLD_STABLE = 10^{-3}$

PERIODIC 2-STEP TRAINING ALGORITHM

TUTTE50 - SEC/2412/60

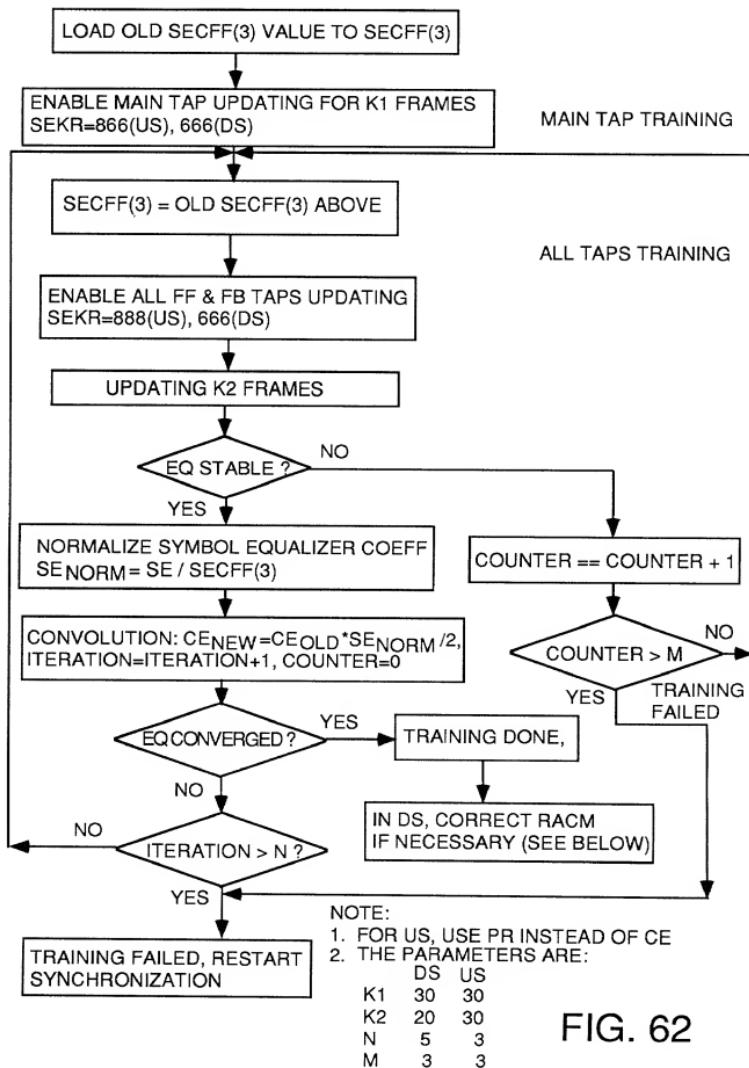
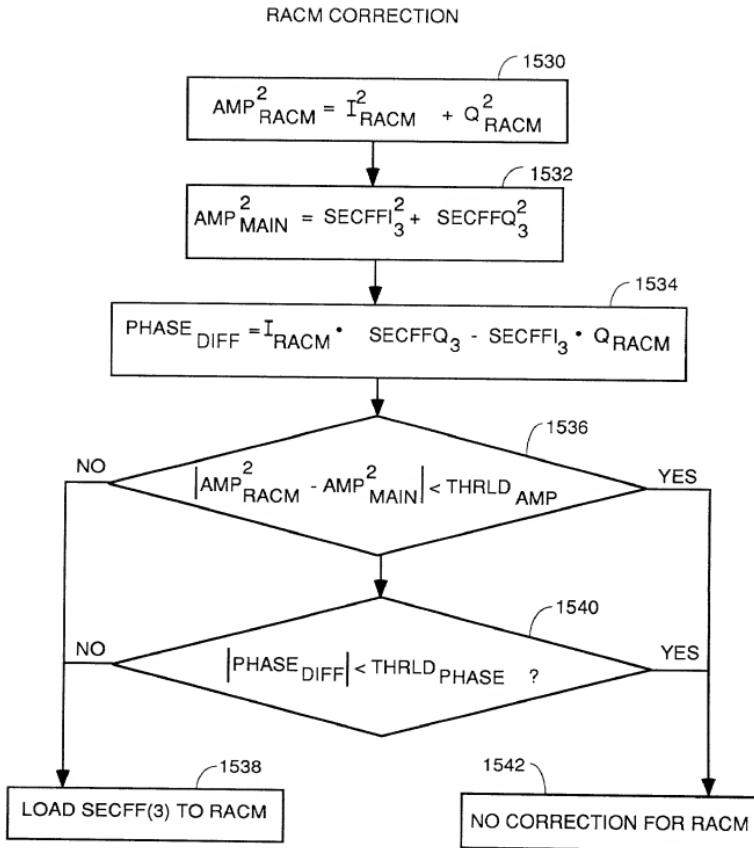


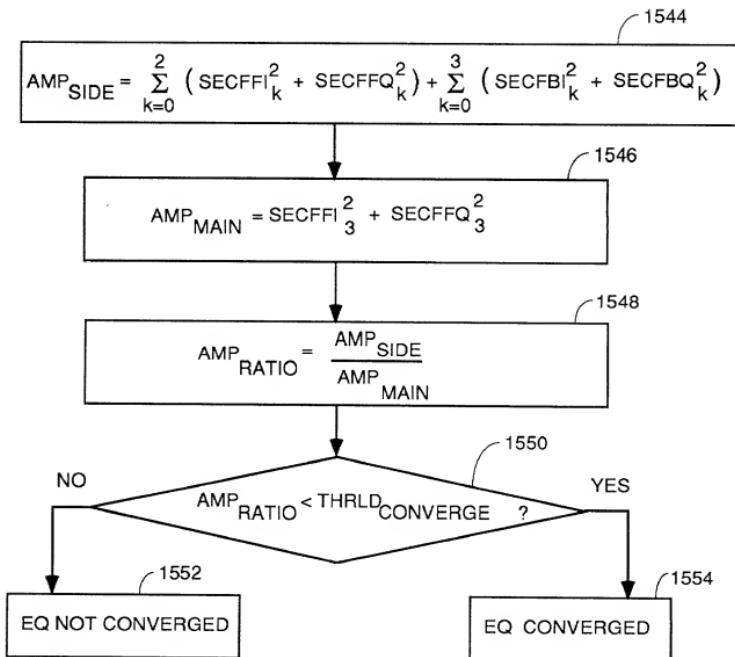
FIG. 62

NOTE: $\text{THRLD}_{\text{AMP}} = \text{TBD}$ $\text{THRLD}_{\text{PHASE}} = \text{TBD}$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

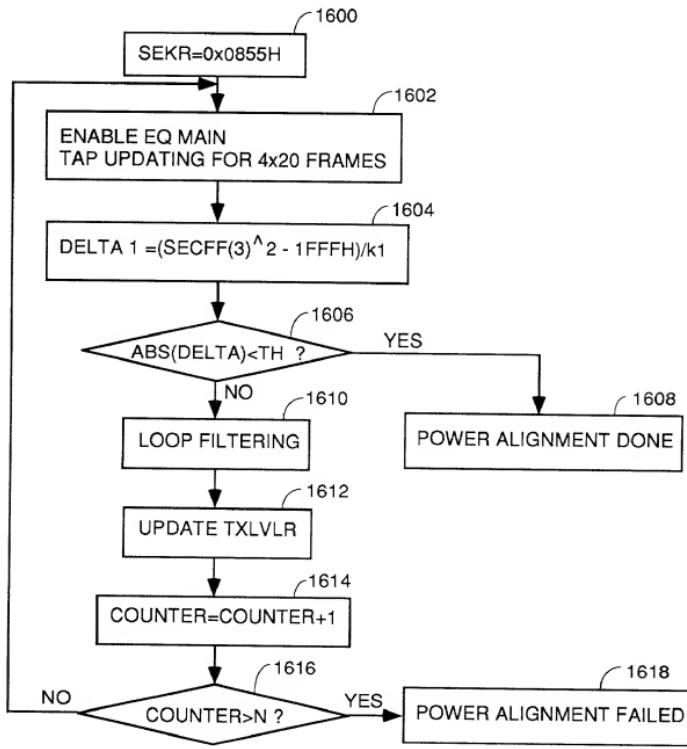
EQ CONVERGENCE CHECK



NOTE: THRLD_{CONVERGE} = 10⁻⁵

FIG. 64

POWER ALIGNMENT FLOW CHART



NOTE: $\text{TH} = 600\text{H}$

$N = 12$

FIG. 65

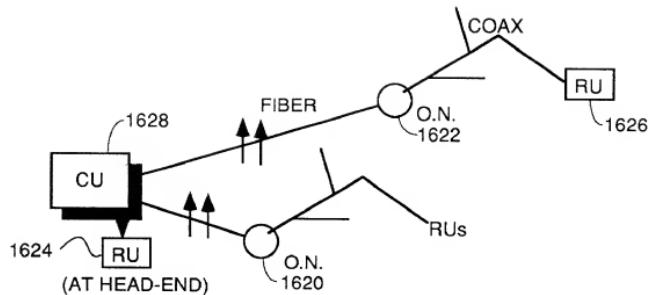
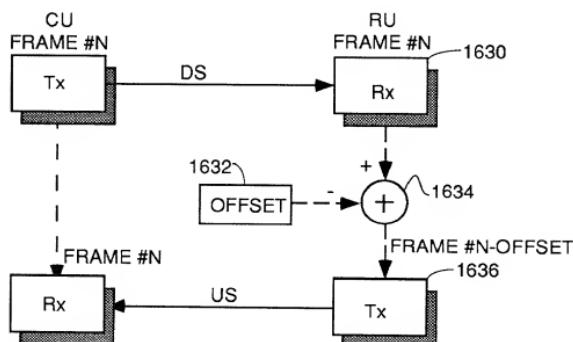


FIG. 66

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TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

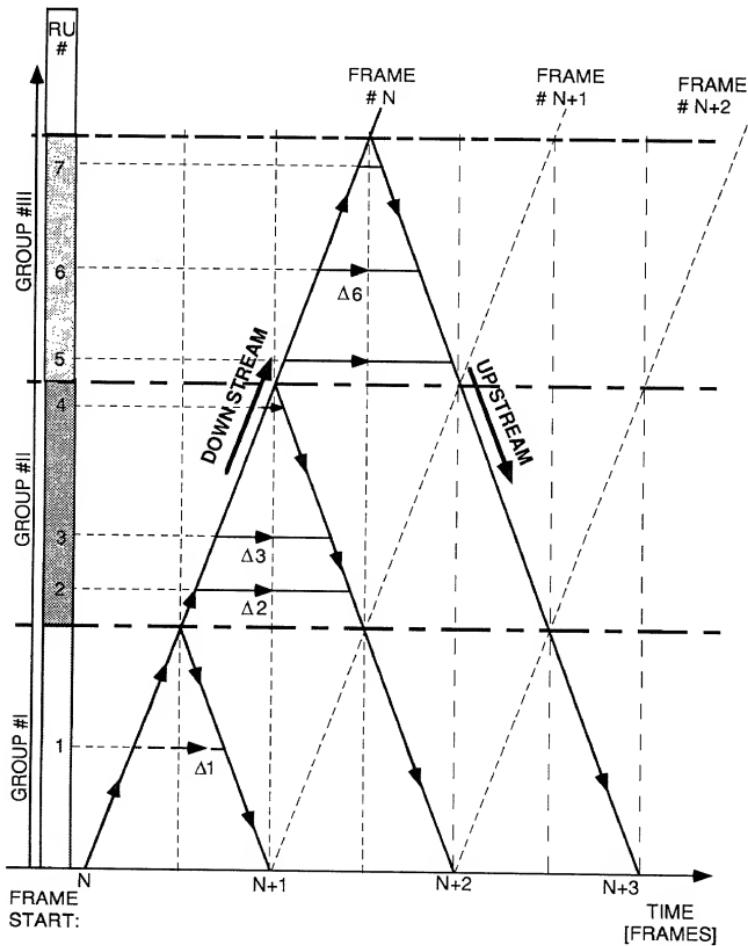
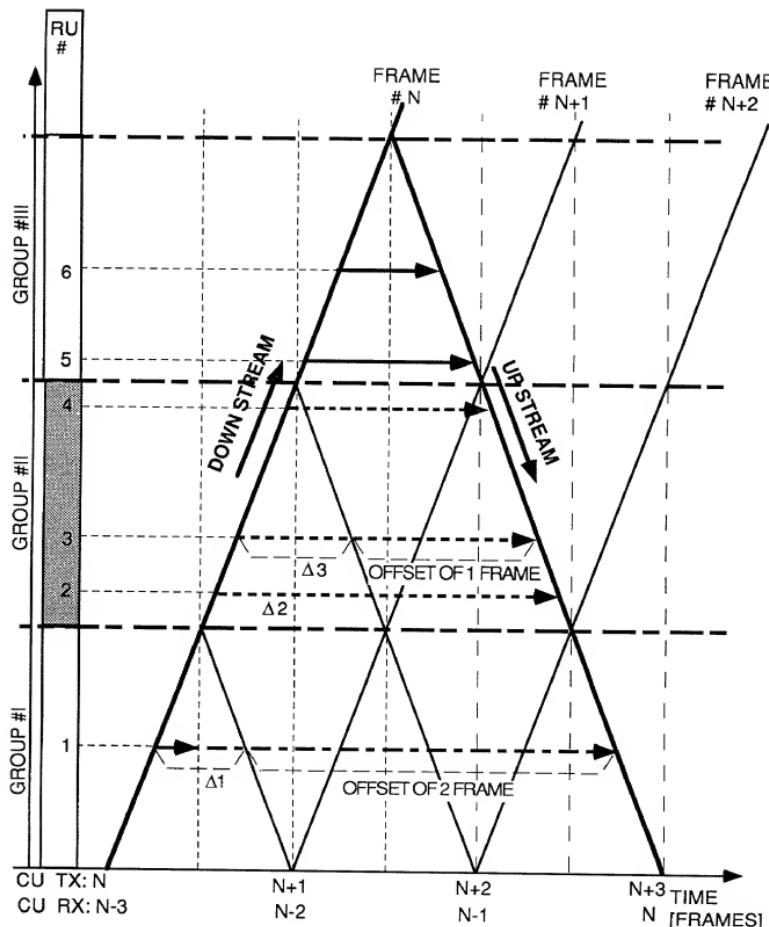


FIG. 68



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM)
PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

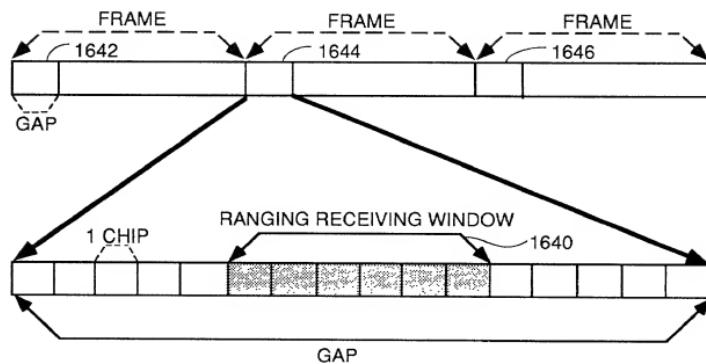


FIG. 70

TO THE "GAPS < 60

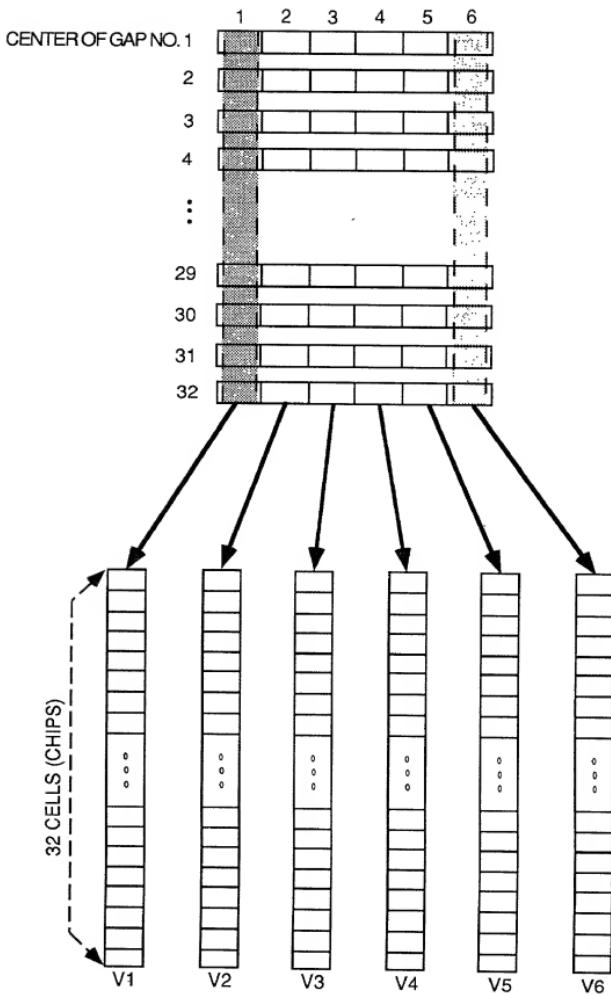


FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	0	0	0	...	

FIG. 72